Radiation Hardened, High Performance Industry Standard Single-Ended Current Mode PWM Controller

ISL78840ASRH, ISL78841ASRH, ISL78843ASRH, ISL78845ASRH

The ISL7884xASRH is a high performance, radiation hardened drop-in replacement for the popular 28C4x and 18C4x PWM controllers suitable for a wide range of power conversion applications including boost, flyback, and isolated output configurations. Its fast signal propagation and output switching characteristics make this an ideal product for existing and new designs.

Features include up to 13.2V operation, low operating current, 90µA typ start-up current, adjustable operating frequency to 1MHz, and high peak current drive capability with 50ns rise and fall times.

PART NUMBER	RISING UVLO	MAX. DUTY CYCLE
ISL78840ASRH	7.0	100%
ISL78841ASRH	7.0	50%
ISL78843ASRH	8.4V	100%
ISL78845ASRH	8.4V	50%

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed in the ordering information must be used when ordering.

Detailed Electrical Specifications for the ISL788xASRH are contained in SMD 5962-07249. A "hot-link" is provided on our website for downloading.

Features

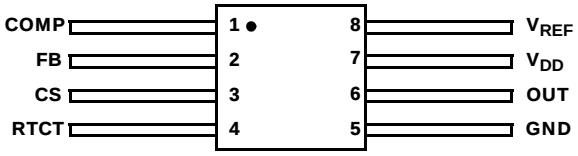
- Electrically Screened to DSCC SMD # 5962-07249
- QML Qualified Per MIL-PRF-38535 Requirements
- 1A MOSFET Gate Driver
- 90µA Typ Start-up Current, 125µA Max
- 35ns Propagation Delay Current Sense to Output
- Fast Transient Response with Peak Current Mode Control
- 9V to 13.2V Operation
- Adjustable Switching Frequency to 1MHz
- 50ns Rise and Fall Times with 1nF Output Load
- Trimmed Timing Capacitor Discharge Current for Accurate Deadtime/Maximum Duty Cycle Control
- 1.5MHz Bandwidth Error Amplifier
- Tight Tolerance Voltage Reference Over Line, Load and Temperature
- ±3% Current Limit Threshold
- Pb-Free Available (RoHS Compliant)

Applications

- Current Mode Switching Power Supplies
- Isolated Buck and Flyback Regulators
- Boost Regulators
- Direction and Speed Control in Motors
- Control of High Current FET Drivers

Pin Configuration

ISL78840ASRH, ISL78841ASRH, ISL78843ASRH, ISL78845ASRH
(8 LD FLATPACK)
TOP VIEW



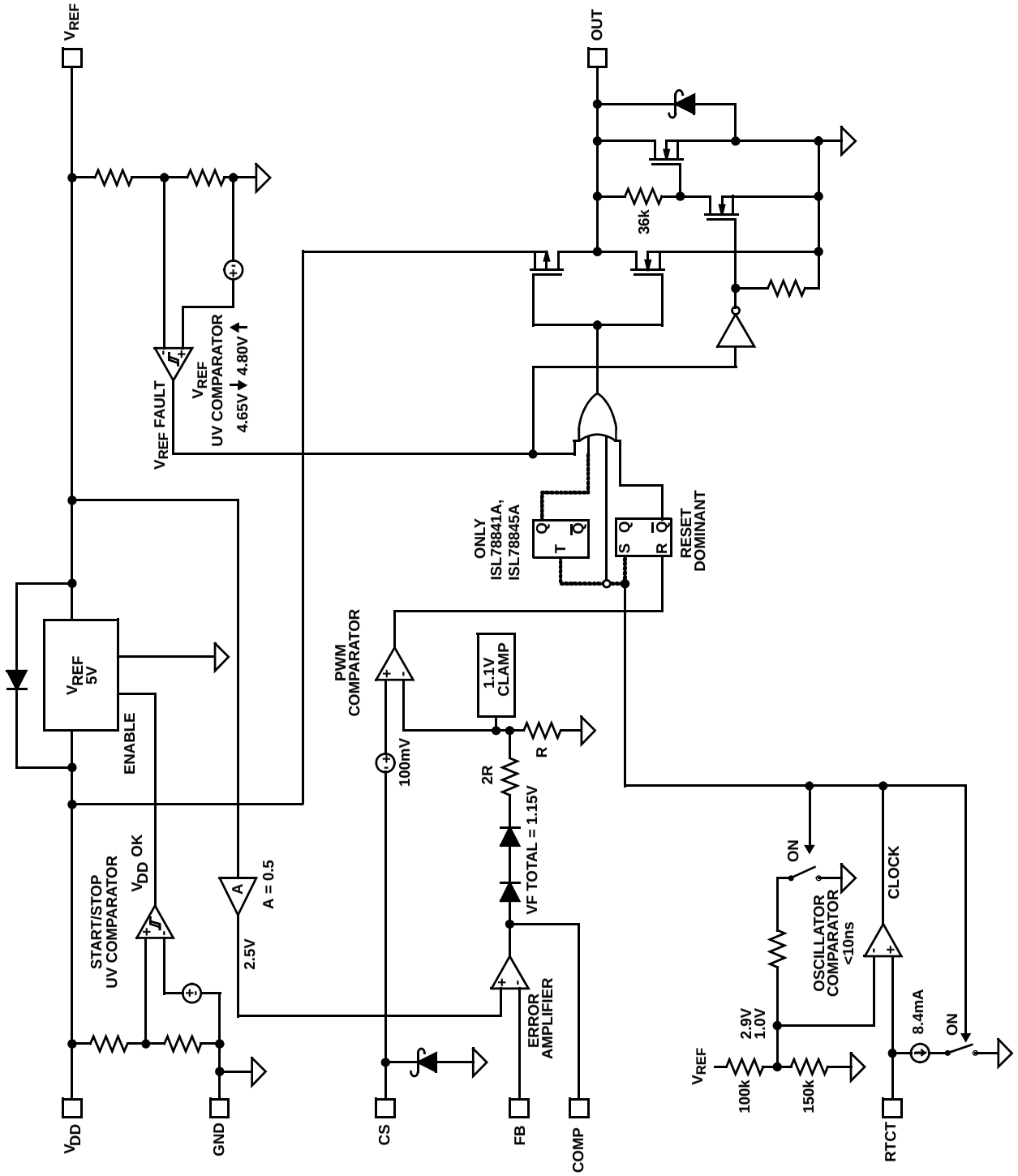
Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (°C)	PACKAGE (Pb-Free)
ISL78840ASRHF/PROTO	ISL78840ASRHF/PROTO (Notes 1, 2)	-55 to +125	8 Ld Flatpack
5962R0724901QXC	ISL78840ASRHQF (Notes 1, 2)	-55 to +125	8 Ld Flatpack
5962R0724901VXC	ISL78840ASRHVF (Notes 1, 2)	-55 to +125	8 Ld Flatpack
ISL78840ASRHVX/SAMPLE	ISL78840ASRHVX/SAMPLE	-55 to +125	Die
ISL78841ASRHF/PROTO	ISL78841ASRHF/PROTO (Notes 1, 2)	-55 to +125	8 Ld Flatpack
5962R0724902QXC	ISL78841ASRHQF (Notes 1, 2)	-55 to +125	8 Ld Flatpack
5962R0724902VXC	ISL78841ASRHVF (Notes 1, 2)	-55 to +125	8 Ld Flatpack
ISL78841ASRHVX/SAMPLE	ISL78841ASRHVX/SAMPLE	-55 to +125	Die
ISL78843ASRHF/PROTO	ISL78843ASRHF/PROTO (Notes 1, 2)	-55 to +125	8 Ld Flatpack
5962R0724903QXC	ISL78843ASRHQF (Notes 1, 2)	-55 to +125	8 Ld Flatpack
5962R0724903VXC	ISL78843ASRHVF (Notes 1, 2)	-55 to +125	8 Ld Flatpack
ISL78843ASRHVX/SAMPLE	ISL78843ASRHVX/SAMPLE	-55 to +125	Die
ISL78845ASRHF/PROTO	ISL78845ASRHF/PROTO (Notes 1, 2)	-55 to +125	8 Ld Flatpack
5962R0724904QXC	ISL78845ASRHQF (Notes 1, 2)	-55 to +125	8 Ld Flatpack
5962R07 24904VXC	ISL78845ASRHVF (Notes 1, 2)	-55 to +125	8 Ld Flatpack
ISL78845ASRHVX/SAMPLE	ISL78845ASRHVX/SAMPLE	-55 to +125	Die

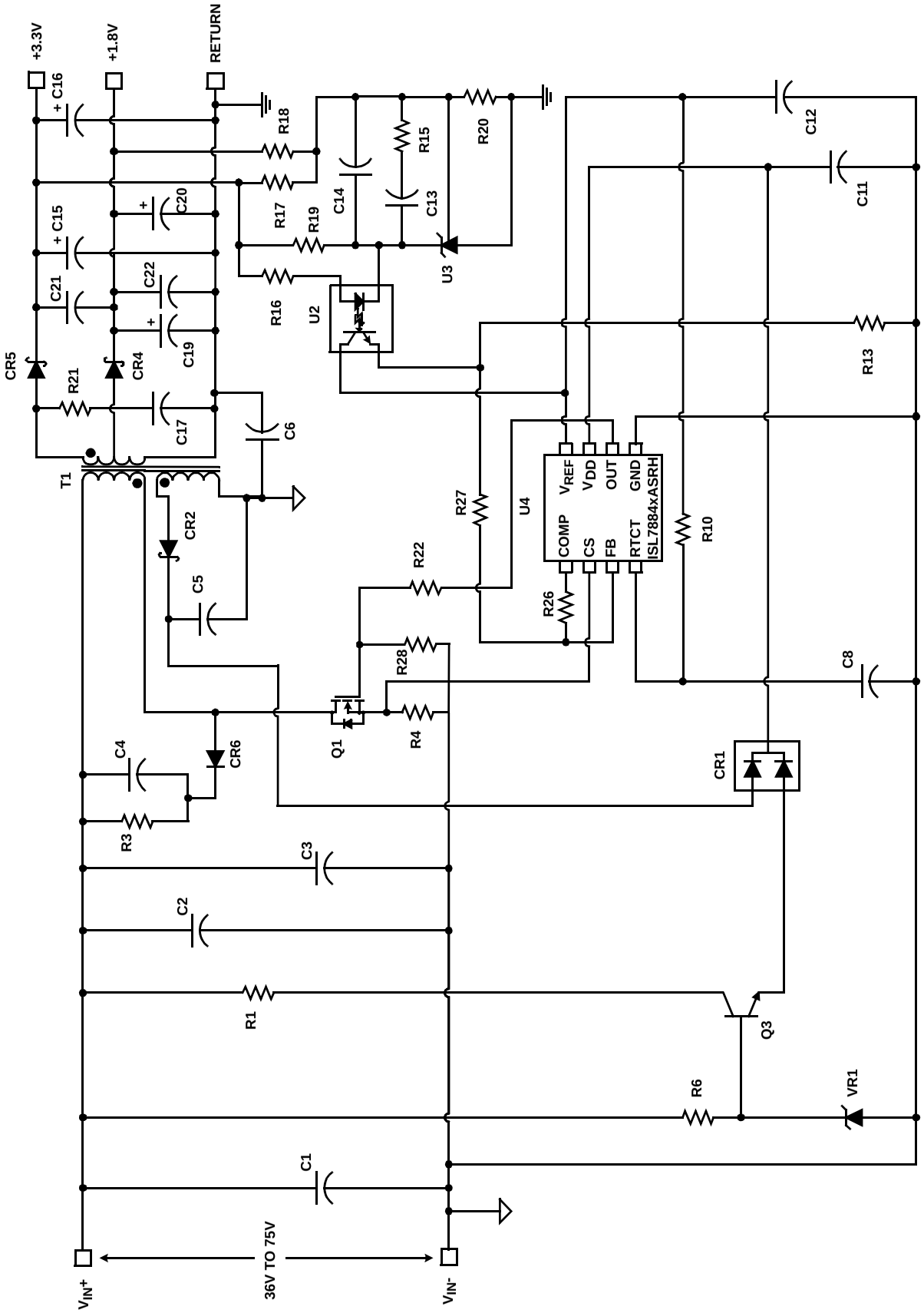
NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISL78840ASRH, ISL78841ASRH, ISL78843ASRH, ISL78845ASRH. For more information on MSL please see techbrief TB363.

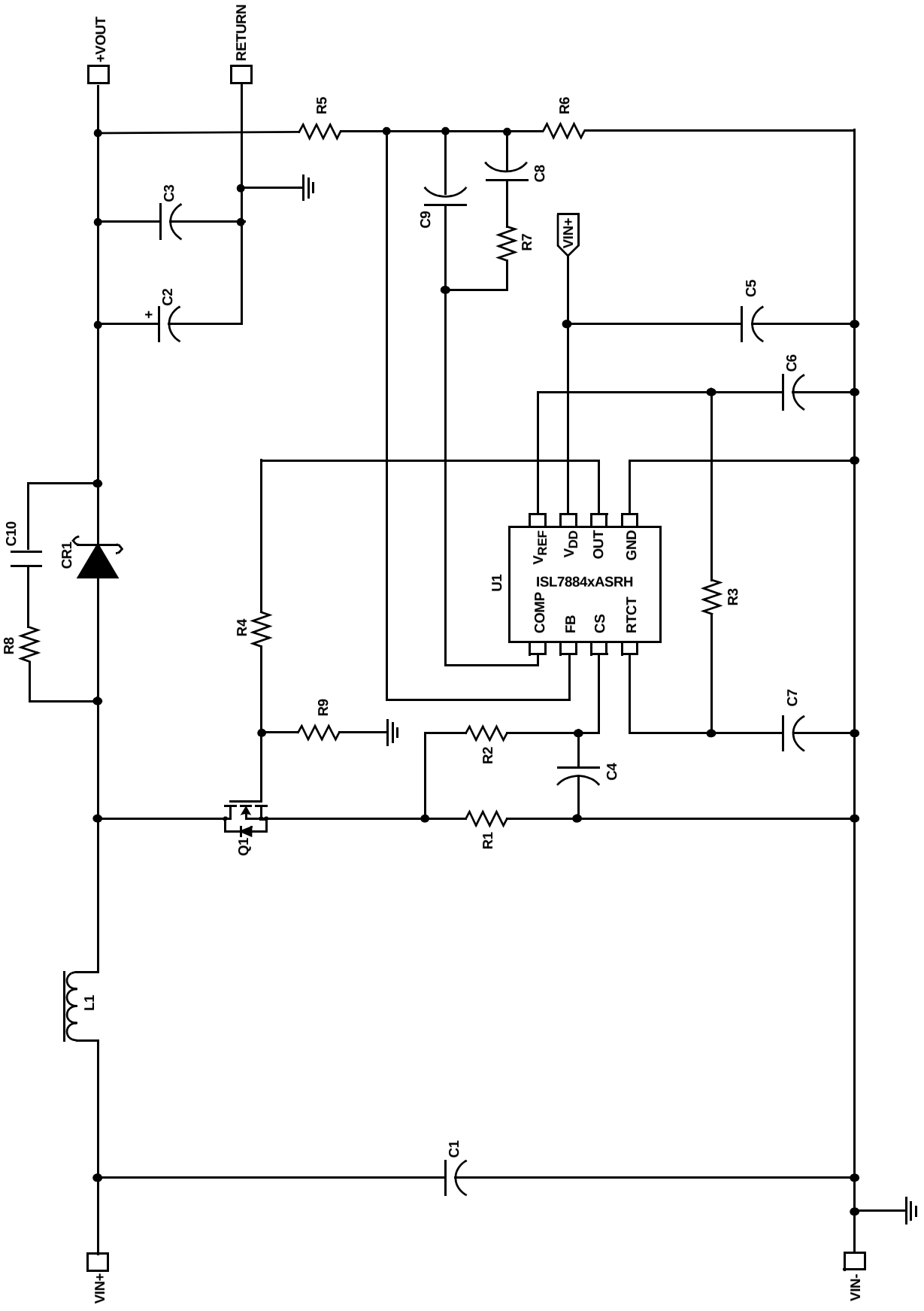
Functional Block Diagram



Typical Application - 48V Input Dual Output Flyback



Typical Application - Boost Converter



Typical Performance Curves

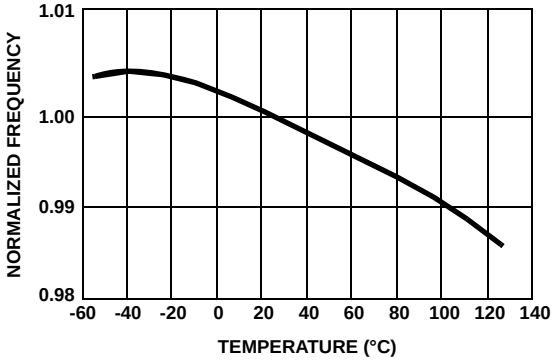


FIGURE 1. FREQUENCY vs TEMPERATURE

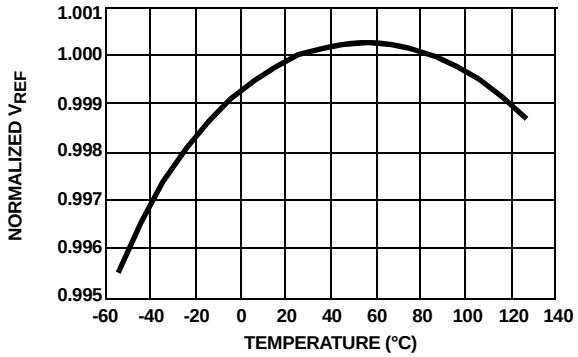


FIGURE 2. REFERENCE VOLTAGE vs TEMPERATURE

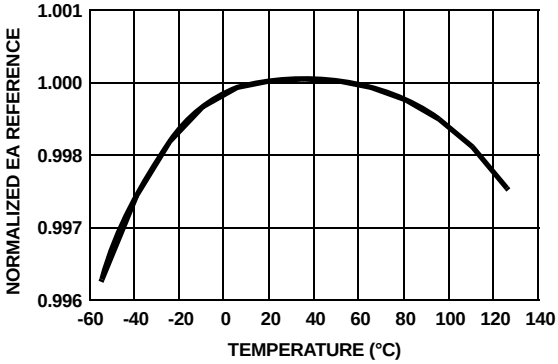


FIGURE 3. EA REFERENCE vs TEMPERATURE

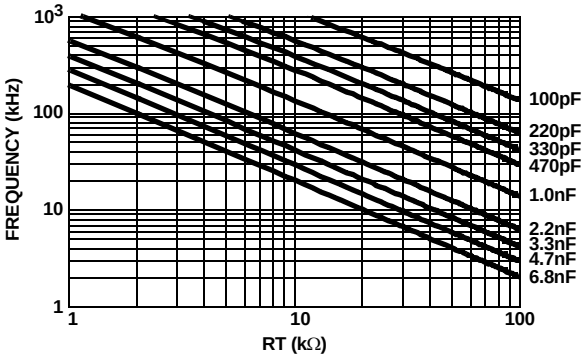


FIGURE 4. RESISTANCE FOR CT CAPACITOR VALUES GIVEN

Pin Descriptions

RTCT - This is the oscillator timing control pin. The operational frequency and maximum duty cycle are set by connecting a resistor, RT, between V_{REF} and this pin and a timing capacitor, CT, from this pin to GND. The oscillator produces a sawtooth waveform with a programmable frequency range up to 2.0MHz. The charge time, t_C, the discharge time, t_D, the switching frequency, f, and the maximum duty cycle, D_{MAX}, can be approximated from the Equations 1 through 4:

$$t_C \approx 0.533 \cdot RT \cdot CT \quad \text{(EQ. 1)}$$

$$t_D \approx -RT \cdot CT \cdot \ln\left(\frac{0.008 \cdot RT - 3.83}{0.008 \cdot RT - 1.71}\right) \quad \text{(EQ. 2)}$$

$$f = 1/(t_C + t_D) \quad \text{(EQ. 3)}$$

$$D = t_C \cdot f \quad \text{(EQ. 4)}$$

The formulae have increased error at higher frequencies due to propagation delays. Figure 4 may be used as a guideline in selecting the capacitor and resistor values required for a given switching frequency for the ISL78841, ISL78845ASRH. The value for the ISL78840, ISL78843ASRH will be twice that shown in Figure 4.

COMP - COMP is the output of the error amplifier and the input of the PWM comparator. The control loop frequency compensation network is connected between the COMP and FB pins.

FB - The output voltage feedback is connected to the inverting input of the error amplifier through this pin. The non-inverting input of the error amplifier is internally tied to a reference voltage.

CS - This is the current sense input to the PWM comparator. The range of the input signal is nominally 0V to 1.0V and has an internal offset of 100mV.

GND - GND is the power and small signal reference ground for all functions.

OUT - This is the drive output to the power switching device. It is a high current output capable of driving the gate of a power MOSFET with peak currents of 1.0A. This GATE output is actively held low when V_{DD} is below the UVLO threshold.

V_{DD} - V_{DD} is the power connection for the device. The total supply current will depend on the load applied to OUT. Total I_{DD} current is the sum of the operating current and the average output current. Knowing the operating frequency, f, and the MOSFET gate charge, Qg,

the average output current can be calculated from Equation 5:

$$I_{OUT} = Qg \times f \quad \text{(EQ. 5)}$$

To optimize noise immunity, bypass V_{DD} to GND with a ceramic capacitor as close to the V_{DD} and GND pins as possible.

V_{REF} - The 5.00V reference voltage output. +1.0/-1.5% tolerance over line, load and operating temperature. The recommended bypass to GND cap is in the range 0.1µF to 0.22µF. A typical value of 0.15µF can be used.

Functional Description

Features

The ISL7884xASRH current mode PWM makes an ideal choice for low-cost flyback and forward topology applications. With its greatly improved performance over industry standard parts, it is the obvious choice for new designs or existing designs which require updating.

Oscillator

The ISL7884xASRH has a sawtooth oscillator with a programmable frequency range to 2MHz, which can be programmed with a resistor from V_{REF} and a capacitor to GND on the RTCT pin. (Please refer to Figure 4 for the resistor and capacitance required for a given frequency).

Soft-Start Operation

Soft-start must be implemented externally. One method, illustrated below, clamps the voltage on COMP.

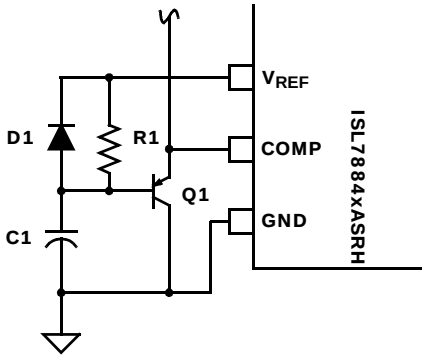


FIGURE 5. SOFT-START

The COMP pin is clamped to the voltage on capacitor C_1 plus a base-emitter junction by transistor Q_1. C_1 is charged from V_{REF} through resistor R_1 and the base current of Q_1. At power-up C_1 is fully discharged, COMP is at ~0.7V, and the duty cycle is zero. As C1 charges, the voltage on COMP increases, and the duty cycle increases in proportion to the voltage on C_1. When COMP reaches the steady state operating point, the control loop takes over and soft start is complete. C_1 continues to charge up to V_{REF} and no longer affects COMP. During power down, diode D1 quickly discharges C1 so that the soft start circuit is properly initialized prior to the next power on sequence.

Gate Drive

The ISL7884xASRH is capable of sourcing and sinking 1A peak current. To limit the peak current through the IC, an optional external resistor may be placed between the totem-pole output of the IC (OUT pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance. TID environment of >50krads requires the use of a bleeder resistor of 10k from OUT pin to GND.

Slope Compensation

For applications where the maximum duty cycle is less than 50%, slope compensation may be used to improve noise immunity, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal. For applications where the duty cycle is greater than 50%, slope compensation is required to prevent instability.

Slope compensation may be accomplished by summing an external ramp with the current feedback signal or by subtracting the external ramp from the voltage feedback error signal. Adding the external ramp to the current feedback signal is the more popular method.

From the small signal current-mode model [1] it can be shown that the naturally-sampled modulator gain, Fm, without slope compensation is calculated in Equation 6:

$$Fm = \frac{1}{SnTsw} \quad \text{(EQ. 6)}$$

where Sn is the slope of the sawtooth signal and tsw is the duration of the half-cycle. When an external ramp is added, the modulator gain becomes Equation 7:

$$Fm = \frac{1}{(Sn + Se)tsw} = \frac{1}{m_c Sntsw} \quad \text{(EQ. 7)}$$

where Se is slope of the external ramp and becomes Equation 8:

$$m_c = 1 + \frac{Se}{Sn} \quad \text{(EQ. 8)}$$

The criteria for determining the correct amount of external ramp can be determined by appropriately setting the damping factor of the double-pole located at the switching frequency. The double-pole will be critically damped if the Q-factor is set to 1, over-damped for Q < 1, and under-damped for Q > 1. An under-damped condition may result in current loop instability.

$$Q = \frac{1}{\pi(m_c(1-D)-0.5)} \quad \text{(EQ. 9)}$$

where D is the percent of on time during a switching cycle. Setting Q = 1 and solving for Se yields Equation 10:

$$S_e = S_n\left(\left(\frac{1}{\pi} + 0.5\right)\frac{1}{1-D} - 1\right) \quad \text{(EQ. 10)}$$

Since Sn and Se are the on time slopes of the current ramp and the external ramp, respectively, they can be multiplied by t_{ON} to obtain the voltage change that occurs during t_{ON}.

$$V_e = V_n\left(\left(\frac{1}{\pi} + 0.5\right)\frac{1}{1-D} - 1\right) \quad \text{(EQ. 11)}$$

where V_n is the change in the current feedback signal (ΔI) during the on time and Ve is the voltage that must be added by the external ramp.

For a flyback converter, Vn can be solved for in terms of input voltage, current transducer components, and primary inductance, yielding Equation 12:

$$V_e = \frac{D \cdot T_{SW} \cdot V_{IN} \cdot R_{CS}}{L_p}\left(\left(\frac{1}{\pi} + 0.5\right)\frac{1}{1-D} - 1\right) \quad V \quad \text{(EQ. 12)}$$

where R_{CS} is the current sense resistor, f_{sw} is the switching frequency, L_p is the primary inductance, V_{IN} is the minimum input voltage, and D is the maximum duty cycle.

The current sense signal at the end of the ON time for CCM operation is Equation 13:

$$V_{CS} = \frac{N_S \cdot R_{CS}}{N_P}\left(I_O + \frac{(1-D) \cdot V_O \cdot f_{sw}}{2L_s}\right) \quad V \quad \text{(EQ. 13)}$$

where V_{CS} is the voltage across the current sense resistor, L_s is the secondary winding inductance, and I_O is the output current at current limit. Equation 13 assumes the voltage drop across the output rectifier is negligible.

Since the peak current limit threshold is 1.00V, the total current feedback signal plus the external ramp voltage must sum to this value when the output load is at the current limit threshold as shown in Equation 14.

$$V_e + V_{CS} = 1 \quad \text{(EQ. 14)}$$

Substituting Equations 12 and 13 into Equation 14 and solving for R_{CS} yields Equation 15:

$$R_{CS} = \frac{1}{\frac{D \cdot f_{sw} \cdot V_{IN}}{L_p} \cdot \left(\frac{\frac{1}{\pi} + 0.5}{1-D} - 1\right) + \frac{N_s}{N_p} \cdot \left(I_O + \frac{(1-D) \cdot V_O \cdot f_{sw}}{2L_s}\right)} \quad \text{(EQ. 15)}$$

Adding slope compensation is accomplished in the ISL7884xASRH using an external buffer transistor and the RTCT signal. A typical application sums the buffered RTCT signal with the current sense feedback and applies the result to the CS pin as shown in Figure 6.

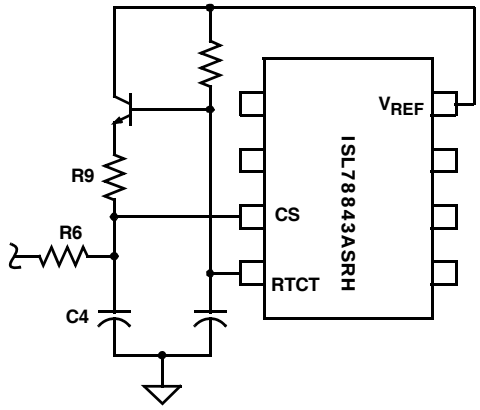


FIGURE 6. SLOPE COMPENSATION

Assuming the designer has selected values for the RC filter (R_6 and C_4) placed on the CS pin, the value of R_9 required to add the appropriate external ramp can be found by superposition.

$$V_e = \frac{2.05D \cdot R_6}{R_6 + R_9} \quad V \quad \text{(EQ. 16)}$$

The factor of 2.05 in Equation 16 arises from the peak amplitude of the sawtooth waveform on RTCT minus a base-emitter junction drop. That voltage multiplied by the maximum duty cycle is the voltage source for the slope compensation. Rearranging to solve for R_9 yields Equation 17:

$$R_9 = \frac{(2.05D - V_e) \cdot R_6}{V_e} \quad \Omega \quad \text{(EQ. 17)}$$

The value of R_{CS} determined in Equation 15 must be rescaled so that the current sense signal presented at the CS pin is that predicted by Equation 13. The divider created by R_6 and R_9 makes this necessary.

$$R'_{CS} = \frac{R_6 + R_9}{R_9} \cdot R_{CS} \quad \text{(EQ. 18)}$$

Example:

V_{IN} = 12V

V_O = 48V

L_s = 800µH

Ns/Np = 10

Lp = 8.0µH

I_O = 200mA

Switching Frequency, f_{sw} = 200kHz

Duty Cycle, D = 28.6%

R_6 = 499Ω

Solve for the current sense resistor, R_{CS}, using Equation 15.

R_{CS} = 295mΩ

Determine the amount of voltage, Ve, that must be added to the current feedback signal using Equation 12.

Ve = 92.4mV

Using Equation 17, solve for the summing resistor, R_9, from CT to CS.

R_9 = 2.67kΩ

Determine the new value of R_{CS} (R'_{CS}) using Equation 18.

R'_{CS} = 350mΩ

Additional slope compensation may be considered for design margin. The above discussion determines the minimum external ramp that is required. The buffer transistor used to create the external ramp from RTCT should have a sufficiently high gain (>200) so as to minimize the required base current. Whatever base current is required reduces the charging current into RTCT and will reduce the oscillator frequency.

Fault Conditions

A Fault condition occurs if V_{REF} falls below 4.65V. When a Fault is detected OUT is disabled. When V_{REF} exceeds 4.80V, the Fault condition clears, and OUT is enabled.

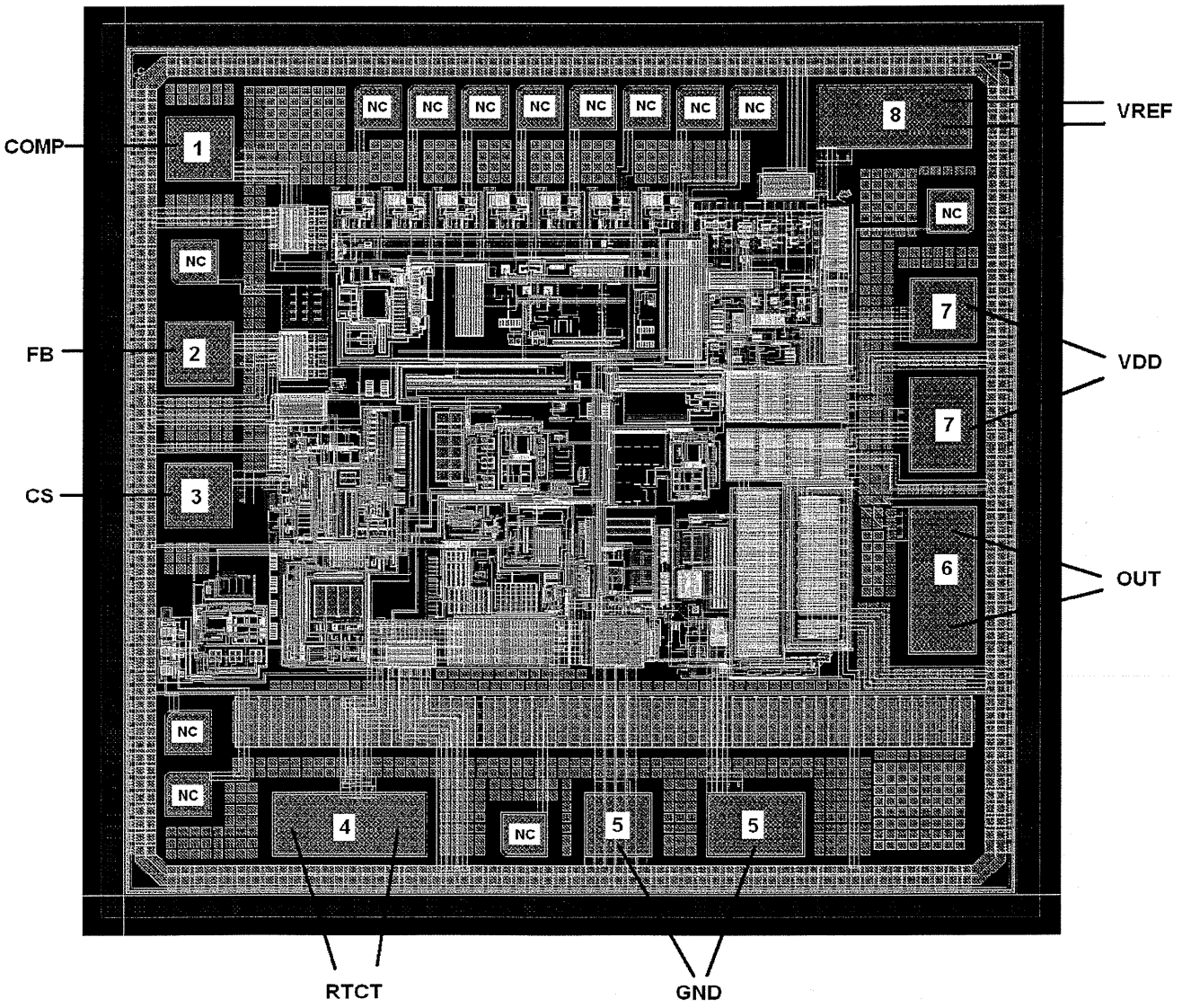
Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. V_{DD} should be bypassed directly to GND with good high frequency capacitors.

References

[1] Ridley, R., “A New Continuous-Time Model for Current Mode Control”, IEEE Transactions on Power Electronics, Vol. 6, No. 2, April 1991.

Die Map


COMP
FB
CS
RTCT
GND
VREF
VDD
OUT
1
2
3
4
5
5
6
7
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NC
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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
12/21/09	FN6991.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL78840ASRH, ISL78841ASRH, ISL78843ASRH, ISL78845ASRH

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php