

# 74AVC1T45

## Dual supply translating transceiver; 3-state

Rev. 02 — 5 May 2009

Product data sheet

## 1. General description

The 74AVC1T45 is a single bit, dual supply transceiver with 3-state output that enables bidirectional level translation. It features one data input-output port (A and B), a direction control input (DIR) and dual supply pins ( $V_{CC(A)}$  and  $V_{CC(B)}$ ). Both  $V_{CC(A)}$  and  $V_{CC(B)}$  can be supplied at any voltage between 0.8 V and 3.6 V making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V). Pins A and DIR are referenced to  $V_{CC(A)}$  and pin B is referenced to  $V_{CC(B)}$ . A HIGH on DIR allows transmission from A to B and a LOW on DIR allows transmission from B to A.

The device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either  $V_{CC(A)}$  or  $V_{CC(B)}$  are at GND level, both A and B are in the high-impedance OFF-state.

## 2. Features

- Wide supply voltage range:
  - ◆  $V_{CC(A)}$ : 0.8 V to 3.6 V
  - ◆  $V_{CC(B)}$ : 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
  - ◆ JESD8-12 (0.8 V to 1.3 V)
  - ◆ JESD8-11 (0.9 V to 1.65 V)
  - ◆ JESD8-7 (1.2 V to 1.95 V)
  - ◆ JESD8-5 (1.8 V to 2.7 V)
  - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114E Class 3B exceeds 8000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101C exceeds 1000 V
- Maximum data rates:
  - ◆ 500 Mbit/s (1.8 V to 3.3 V translation)
  - ◆ 320 Mbit/s (< 1.8 V to 3.3 V translation)
  - ◆ 320 Mbit/s (translate to 2.5 V or 1.8 V)
  - ◆ 280 Mbit/s (translate to 1.5 V)
  - ◆ 240 Mbit/s (translate to 1.2 V)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II

- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V<sub>CC</sub>
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVC1T45GW	−40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363
74AVC1T45GM	−40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886

4. Marking

Table 2. Marking

Type number	Marking code <sup>[1]</sup>
74AVC1T45GW	B5
74AVC1T45GM	B5

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

001aag885

**Fig 1. Logic symbol**

001aag886

**Fig 2. Logic diagram**

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
V <sub>CC(A)</sub>	1	supply voltage port A and DIR
GND	2	ground (0 V)
A	3	data input or output
B	4	data input or output
DIR	5	direction control
V <sub>CC(B)</sub>	6	supply voltage port B

7. Functional description

Table 4. Function table<sup>[1]</sup>

Supply voltage	Input	Input/output <sup>[2]</sup>	
V <sub>CC(A)</sub> , V <sub>CC(B)</sub>	DIR <sup>[3]</sup>	A	B
0.8 V to 3.6 V	L	A = B	input
0.8 V to 3.6 V	H	input	B = A
GND <sup>[4]</sup>	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The input circuit of the data I/O is always active.

[3] The DIR input circuit is referenced to V<sub>CC(A)</sub>.

[4] When either V<sub>CC(A)</sub> or V<sub>CC(B)</sub> is at GND level, the device goes into suspend mode.

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage port A		-0.5	+4.6	V
$V_{CC(B)}$	supply voltage port B		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		[1] -0.5	+4.6	V
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$V_O$	output voltage	Active mode	[1][2][3] -0.5	$V_{CCO} + 0.5$	V
		Suspend or 3-state mode	[1] -0.5	+4.6	V
$I_O$	output current	$V_O = 0$ V to $V_{CCO}$	-	$\pm 50$	mA
$I_{CC}$	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[4] -	250	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.

[3]  $V_{CCO} + 0.5$  V should not exceed 4.6 V.

[4] For SC-88 packages: above 87.5 °C the value of  $P_{tot}$  derates linearly with 4.0 mW/K.  
For XSON6 package: above 118 °C the value of  $P_{tot}$  derates linearly with 7.8 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		0.8	3.6	V
$V_{CC(B)}$	supply voltage B		0.8	3.6	V
$V_I$	input voltage		0	3.6	V
$V_O$	output voltage	Active mode	[1] 0	$V_{CCO}$	V
		Suspend or 3-state mode	0	3.6	V
$T_{amb}$	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CCI} = 0.8$ V to 3.6 V	[2] -	5	ns/V

[1]  $V_{CCO}$  is the supply voltage associated with the output port.

[2]  $V_{CCI}$  is the supply voltage associated with the input port.

## 10. Static characteristics

**Table 7. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = 25 °C</b>						
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -1.5 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V	-	0.69	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 1.5 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V	-	0.07	-	V
I <sub>I</sub>	input leakage current	DIR input; V <sub>I</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±0.025	±0.25	μA
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	[1] -	±0.5	±2.5	μA
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±0.1	±1	μA
		B port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0.8 V to 3.6 V	-	±0.1	±1	μA
C <sub>I</sub>	input capacitance	DIR input; V <sub>I</sub> = 0 V or 3.3 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.3 V	-	1	-	pF
C <sub>I/O</sub>	input/output capacitance	A and B port; suspend mode; V <sub>O</sub> = 3.3 V or 0 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.3 V	-	4	-	pF
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	data input [2]				
		V <sub>CCI</sub> = 0.8 V	0.70V <sub>CCI</sub>	-	-	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	0.65V <sub>CCI</sub>	-	-	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	2	-	-	V
		DIR input				
		V <sub>CCI</sub> = 0.8 V	0.70V <sub>CC(A)</sub>	-	-	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	0.65V <sub>CC(A)</sub>	-	-	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	2	-	-	V
V <sub>IL</sub>	LOW-level input voltage	data input [2]				
		V <sub>CCI</sub> = 0.8 V	-	-	0.30V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	-	-	0.35V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	-	-	0.9	V
		DIR input				
		V <sub>CCI</sub> = 0.8 V	-	-	0.30V <sub>CC(A)</sub>	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	-	-	0.35V <sub>CC(A)</sub>	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	-	-	0.9	V

**Table 7.** Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -100\ \mu\text{A}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\ \text{V to } 3.6\ \text{V}$	[1] $V_{CCO} - 0.1$	-	-	V
		$I_O = -3\ \text{mA}$ ; $V_{CC(A)} = V_{CC(B)} = 1.1\ \text{V}$	0.85	-	-	V
		$I_O = -6\ \text{mA}$ ; $V_{CC(A)} = V_{CC(B)} = 1.4\ \text{V}$	1.05	-	-	V
		$I_O = -8\ \text{mA}$ ; $V_{CC(A)} = V_{CC(B)} = 1.65\ \text{V}$	1.2	-	-	V
		$I_O = -9\ \text{mA}$ ; $V_{CC(A)} = V_{CC(B)} = 2.3\ \text{V}$	1.75	-	-	V
		$I_O = -12\ \text{mA}$ ; $V_{CC(A)} = V_{CC(B)} = 3.0\ \text{V}$	2.3	-	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 100\ \mu\text{A}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\ \text{V to } 3.6\ \text{V}$	-	-	0.1	V
		$I_O = 3\ \text{mA}$ ; $V_{CC(A)} = V_{CC(B)} = 1.1\ \text{V}$	-	-	0.25	V
		$I_O = 6\ \text{mA}$ ; $V_{CC(A)} = V_{CC(B)} = 1.4\ \text{V}$	-	-	0.35	V
		$I_O = 8\ \text{mA}$ ; $V_{CC(A)} = V_{CC(B)} = 1.65\ \text{V}$	-	-	0.45	V
		$I_O = 9\ \text{mA}$ ; $V_{CC(A)} = V_{CC(B)} = 2.3\ \text{V}$	-	-	0.55	V
		$I_O = 12\ \text{mA}$ ; $V_{CC(A)} = V_{CC(B)} = 3.0\ \text{V}$	-	-	0.7	V
$I_I$	input leakage current	DIR input; $V_I = 0\ \text{V to } 3.6\ \text{V}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\ \text{V to } 3.6\ \text{V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0\ \text{V or } V_{CCO}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\ \text{V to } 3.6\ \text{V}$	[1] -	-	$\pm 5$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0\ \text{V to } 3.6\ \text{V}$ ; $V_{CC(A)} = 0\ \text{V}$ ; $V_{CC(B)} = 0.8\ \text{V to } 3.6\ \text{V}$	-	-	$\pm 5$	$\mu\text{A}$
		B port; $V_I$ or $V_O = 0\ \text{V to } 3.6\ \text{V}$ ; $V_{CC(B)} = 0\ \text{V}$ ; $V_{CC(A)} = 0.8\ \text{V to } 3.6\ \text{V}$	-	-	$\pm 5$	$\mu\text{A}$
$I_{CC}$	supply current	A port; $V_I = 0\ \text{V or } V_{CCI}$ ; $I_O = 0\ \text{A}$	[2]			
		$V_{CC(A)} = 0.8\ \text{V to } 3.6\ \text{V}$ ; $V_{CC(B)} = 0.8\ \text{V to } 3.6\ \text{V}$	-	-	8.0	$\mu\text{A}$
		$V_{CC(A)} = 3.6\ \text{V}$ ; $V_{CC(B)} = 0\ \text{V}$	-	-	8.0	$\mu\text{A}$
		$V_{CC(A)} = 0\ \text{V}$ ; $V_{CC(B)} = 3.6\ \text{V}$	-2	0	-	$\mu\text{A}$
		B port; $V_I = 0\ \text{V or } V_{CCI}$ ; $I_O = 0\ \text{A}$	[2]			
		$V_{CC(A)} = 0.8\ \text{V to } 3.6\ \text{V}$ ; $V_{CC(B)} = 0.8\ \text{V to } 3.6\ \text{V}$	-	-	8.0	$\mu\text{A}$
		$V_{CC(A)} = 3.6\ \text{V}$ ; $V_{CC(B)} = 0\ \text{V}$	-2	0	-	$\mu\text{A}$
		$V_{CC(A)} = 0\ \text{V}$ ; $V_{CC(B)} = 3.6\ \text{V}$	-	-	8.0	$\mu\text{A}$
		A plus B port ( $I_{CC(A)} + I_{CC(B)}$ ); $I_O = 0\ \text{A}$ ; $V_I = \text{GND or } V_{CCI}$ ; $V_{CC(A)} = 0.8\ \text{V to } 3.6\ \text{V}$ ; $V_{CC(B)} = 0.8\ \text{V to } 3.6\ \text{V}$	[2] -	-	16	$\mu\text{A}$

**Table 7.** Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	data input	[2]			
		V <sub>CCI</sub> = 0.8 V	0.70V <sub>CCI</sub>	-	-	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	0.65V <sub>CCI</sub>	-	-	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	2	-	-	V
		DIR input				
		V <sub>CCI</sub> = 0.8 V	0.70V <sub>CC(A)</sub>	-	-	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	0.65V <sub>CC(A)</sub>	-	-	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	2	-	-	V
V <sub>IL</sub>	LOW-level input voltage	data input	[2]			
		V <sub>CCI</sub> = 0.8 V	-	-	0.30V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	-	-	0.35V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	-	-	0.9	V
		DIR input				
		V <sub>CCI</sub> = 0.8 V	-	-	0.30V <sub>CC(A)</sub>	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	-	-	0.35V <sub>CC(A)</sub>	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	-	-	0.9	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 µA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	[1] V <sub>CCO</sub> - 0.1	-	-	V
		I <sub>O</sub> = -3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	0.85	-	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	1.05	-	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	1.2	-	-	V
		I <sub>O</sub> = -9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	1.75	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	2.3	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 µA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	-	0.1	V
		I <sub>O</sub> = 3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	-	-	0.25	V
		I <sub>O</sub> = 6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	-	-	0.35	V
		I <sub>O</sub> = 8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	-	-	0.45	V
		I <sub>O</sub> = 9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	-	-	0.55	V
		I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	-	-	0.7	V
I <sub>I</sub>	input leakage current	DIR input; V <sub>I</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	-	±1.5	µA
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	[1] -	-	±7.5	µA

**Table 7.** Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0$ V to 3.6 V; $V_{CC(B)} = 0$ V; $V_{CC(A)} = 0.8$ V to 3.6 V	-	-	$\pm 35$	$\mu$ A
		B port; $V_I$ or $V_O = 0$ V to 3.6 V; $V_{CC(B)} = 0$ V; $V_{CC(A)} = 0.8$ V to 3.6 V	-	-	$\pm 35$	$\mu$ A
$I_{CC}$	supply current	A port; $V_I = 0$ V or $V_{CCI}$ ; $I_O = 0$ A	[2]			
		$V_{CC(A)} = 0.8$ V to 3.6 V; $V_{CC(B)} = 0.8$ V to 3.6 V	-	-	12	$\mu$ A
		$V_{CC(A)} = 3.6$ V; $V_{CC(B)} = 0$ V	-	-	12	$\mu$ A
		$V_{CC(A)} = 0$ V; $V_{CC(B)} = 3.6$ V	-8	0	-	$\mu$ A
		B port; $V_I = 0$ V or $V_{CCI}$ ; $I_O = 0$ A	[2]			
		$V_{CC(A)} = 0.8$ V to 3.6 V; $V_{CC(B)} = 0.8$ V to 3.6 V	-	-	12	$\mu$ A
		$V_{CC(A)} = 3.6$ V; $V_{CC(B)} = 0$ V	-8	0	-	$\mu$ A
		$V_{CC(A)} = 0$ V; $V_{CC(B)} = 3.6$ V	-	-	12	$\mu$ A
		A plus B port ( $I_{CC(A)} + I_{CC(B)}$ ); $I_O = 0$ A; $V_I = \text{GND}$ or $V_{CCI}$ ; $V_{CC(A)} = 0.8$ V to 3.6 V; $V_{CC(B)} = 0.8$ V to 3.6 V	[2]	-	24	$\mu$ A

[1]  $V_{CCO}$  is the supply voltage associated with the output port.[2]  $V_{CCI}$  is the supply voltage associated with the data input port.



## 11. Dynamic characteristics

**Table 8. Typical dynamic characteristics at  $V_{CC(A)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$  [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#)

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	A to B	15.5	8.1	7.6	7.7	8.4	9.2	ns
		B to A	15.5	12.7	12.3	12.2	12.0	11.8	ns
$t_{dis}$	disable time	DIR to A	12.2	12.2	12.2	12.2	12.2	12.2	ns
		DIR to B	11.7	7.9	7.6	8.2	8.7	10.2	ns
$t_{en}$	enable time	DIR to A	27.2	20.6	19.9	20.4	20.7	22.0	ns
		DIR to B	27.7	20.3	19.8	19.9	20.6	21.4	ns

- [1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{en}$  is a calculated value using the formula shown in [Section 13.4 "Enable times"](#)

**Table 9. Typical dynamic characteristics at  $V_{CC(B)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ °C}$  [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#)

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	A to B	15.5	12.7	12.3	12.2	12.0	11.8	ns
		B to A	15.5	8.1	7.6	7.7	8.4	9.2	ns
$t_{dis}$	disable time	DIR to A	12.2	4.9	3.8	3.7	2.8	3.4	ns
		DIR to B	11.7	9.2	9.0	8.8	8.7	8.6	ns
$t_{en}$	enable time	DIR to A	27.2	17.3	16.6	16.5	17.1	17.8	ns
		DIR to B	27.7	17.6	16.1	15.9	14.8	15.2	ns

- [1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{en}$  is a calculated value using the formula shown in [Section 13.4 "Enable times"](#)

**Table 10. Typical power dissipation capacitance at  $V_{CC(A)} = V_{CC(B)}$  and  $T_{amb} = 25\text{ °C}$  [1][2]**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)}$ and $V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$C_{PD}$	power dissipation capacitance	A port: (direction A to B); B port: (direction B to A)	1	2	2	2	2	2	pF
		A port: (direction B to A); B port: (direction A to B)	9	11	11	12	14	17	pF

- [1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

- [2]  $f_i = 10\text{ MHz}$ ;  $V_i = \text{GND to } V_{CC}$ ;  $t_r = t_f = 1\text{ ns}$ ;  $C_L = 0\text{ pF}$ ;  $R_L = \infty\text{ }\Omega$ .

**Table 11. Dynamic characteristics for temperature range –40 °C to +85 °C [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#).

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>CC(A)</sub> = 1.1 V to 1.3 V													
t <sub>pd</sub>	propagation delay	A to B	1.0	9.0	0.7	6.8	0.6	6.1	0.5	5.7	0.5	6.1	ns
		B to A	1.0	9.0	0.8	8.0	0.7	7.7	0.6	7.2	0.5	7.1	ns
t <sub>dis</sub>	disable time	DIR to A	2.2	8.8	2.2	8.8	2.2	8.8	2.2	8.8	2.2	8.8	ns
		DIR to B	2.2	8.4	1.8	6.7	2.0	6.9	1.7	6.2	2.4	7.2	ns
t <sub>en</sub>	enable time	DIR to A	-	17.4	-	14.7	-	14.6	-	13.4	-	14.3	ns
		DIR to B	-	17.8	-	15.6	-	14.9	-	14.5	-	14.9	ns
V <sub>CC(A)</sub> = 1.4 V to 1.6 V													
t <sub>pd</sub>	propagation delay	A to B	1.0	8.0	0.7	5.4	0.6	4.6	0.5	3.7	0.5	3.5	ns
		B to A	1.0	6.8	0.8	5.4	0.7	5.1	0.6	4.7	0.5	4.5	ns
t <sub>dis</sub>	disable time	DIR to A	1.6	6.3	1.6	6.3	1.6	6.3	1.6	6.3	1.6	6.3	ns
		DIR to B	2.0	7.6	1.8	5.9	1.6	6.0	1.2	4.8	1.7	5.5	ns
t <sub>en</sub>	enable time	DIR to A	-	14.4	-	11.3	-	11.1	-	9.5	-	10.0	ns
		DIR to B	-	14.3	-	11.7	-	10.9	-	10.0	-	9.8	ns
V <sub>CC(A)</sub> = 1.65 V to 1.95 V													
t <sub>pd</sub>	propagation delay	A to B	1.0	7.7	0.6	5.1	0.5	4.3	0.5	3.4	0.5	3.1	ns
		B to A	1.0	6.1	0.7	4.6	0.5	4.4	0.5	3.9	0.5	3.7	ns
t <sub>dis</sub>	disable time	DIR to A	1.6	5.5	1.6	5.5	1.6	5.5	1.6	5.5	1.6	5.5	ns
		DIR to B	1.8	7.7	1.8	5.7	1.4	5.8	1.0	4.5	1.5	5.2	ns
t <sub>en</sub>	enable time	DIR to A	-	13.8	-	10.3	-	10.2	-	8.4	-	8.9	ns
		DIR to B	-	13.2	-	10.6	-	9.8	-	8.9	-	8.6	ns
V <sub>CC(A)</sub> = 2.3 V to 2.7 V													
t <sub>pd</sub>	propagation delay	A to B	1.0	7.2	0.5	4.7	0.5	3.9	0.5	3.0	0.5	2.6	ns
		B to A	1.0	5.7	0.6	3.8	0.5	3.4	0.5	3.0	0.5	2.8	ns
t <sub>dis</sub>	disable time	DIR to A	1.5	4.2	1.5	4.2	1.5	4.2	1.5	4.2	1.5	4.2	ns
		DIR to B	1.7	7.3	2.0	5.2	1.5	5.1	0.6	4.2	1.1	4.8	ns
t <sub>en</sub>	enable time	DIR to A	-	13.0	-	9.0	-	8.5	-	7.2	-	7.6	ns
		DIR to B	-	11.4	-	8.9	-	8.1	-	7.2	-	6.8	ns
V <sub>CC(A)</sub> = 3.0 V to 3.6 V													
t <sub>pd</sub>	propagation delay	A to B	1.0	7.1	0.5	4.5	0.5	3.7	0.5	2.8	0.5	2.4	ns
		B to A	1.0	6.1	0.6	3.6	0.5	3.1	0.5	2.6	0.5	2.4	ns
t <sub>dis</sub>	disable time	DIR to A	1.5	4.7	1.5	4.7	1.5	4.7	1.5	4.7	1.5	4.7	ns
		DIR to B	1.7	7.2	0.7	5.5	0.6	5.5	0.7	4.1	1.7	4.7	ns
t <sub>en</sub>	enable time	DIR to A	-	13.3	-	9.1	-	8.6	-	6.7	-	7.1	ns
		DIR to B	-	11.8	-	9.2	-	8.4	-	7.5	-	7.1	ns

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
t<sub>en</sub> is a calculated value using the formula shown in [Section 13.4 "Enable times"](#)

**Table 12. Dynamic characteristics for temperature range –40 °C to +125 °C [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#); for wave forms see [Figure 5](#) and [Figure 6](#)

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>CC(A)</sub> = 1.1 V to 1.3 V													
t <sub>pd</sub>	propagation delay	A to B	1.0	9.9	0.7	7.5	0.6	6.8	0.5	6.3	0.5	6.8	ns
		B to A	1.0	9.9	0.8	8.8	0.7	8.5	0.6	8.0	0.5	7.9	ns
t <sub>dis</sub>	disable time	DIR to A	2.2	9.7	2.2	9.7	2.2	9.7	2.2	9.7	2.2	9.7	ns
		DIR to B	2.2	9.2	1.8	7.4	2.0	7.6	1.7	6.9	2.4	8.0	ns
t <sub>en</sub>	enable time	DIR to A	-	19.1	-	16.2	-	16.1	-	14.9	-	15.9	ns
		DIR to B	-	19.6	-	17.2	-	16.5	-	16.0	-	16.5	ns
V <sub>CC(A)</sub> = 1.4 V to 1.6 V													
t <sub>pd</sub>	propagation delay	A to B	1.0	8.8	0.7	6.0	0.6	5.1	0.5	4.1	0.5	3.9	ns
		B to A	1.0	7.5	0.8	6.0	0.7	5.7	0.6	5.2	0.5	5.0	ns
t <sub>dis</sub>	disable time	DIR to A	1.6	7.0	1.6	7.0	1.6	7.0	1.6	7.0	1.6	7.0	ns
		DIR to B	2.0	8.3	1.8	6.5	1.6	6.6	1.2	5.3	1.7	6.1	ns
t <sub>en</sub>	enable time	DIR to A	-	15.8	-	12.5	-	12.3	-	10.5	-	11.1	ns
		DIR to B	-	15.8	-	13.0	-	12.1	-	11.1	-	10.9	ns
V <sub>CC(A)</sub> = 1.65 V to 1.95 V													
t <sub>pd</sub>	propagation delay	A to B	1.0	8.5	0.6	5.7	0.5	4.8	0.5	3.8	0.5	3.5	ns
		B to A	1.0	6.8	0.7	5.1	0.5	4.9	0.5	4.3	0.5	4.1	ns
t <sub>dis</sub>	disable time	DIR to A	1.6	6.1	1.6	6.1	1.6	6.1	1.6	6.1	1.6	6.1	ns
		DIR to B	1.8	8.5	1.8	6.3	1.4	6.4	1.0	5.0	1.5	5.8	ns
t <sub>en</sub>	enable time	DIR to A	-	15.3	-	11.4	-	11.3	-	9.3	-	9.9	ns
		DIR to B	-	14.6	-	11.8	-	10.9	-	9.9	-	9.6	ns
V <sub>CC(A)</sub> = 2.3 V to 2.7 V													
t <sub>pd</sub>	propagation delay	A to B	1.0	8.0	0.5	5.2	0.5	4.3	0.5	3.3	0.5	2.9	ns
		B to A	1.0	6.3	0.6	4.2	0.5	3.8	0.5	3.3	0.5	3.1	ns
t <sub>dis</sub>	disable time	DIR to A	1.5	4.7	1.5	4.7	1.5	4.7	1.5	4.7	1.5	4.7	ns
		DIR to B	1.7	8.0	2.0	5.8	1.5	5.7	0.6	4.7	1.1	5.3	ns
t <sub>en</sub>	enable time	DIR to A	-	14.3	-	10.0	-	9.5	-	8.0	-	8.4	ns
		DIR to B	-	12.7	-	9.9	-	9.0	-	8.0	-	7.6	ns
V <sub>CC(A)</sub> = 3.0 V to 3.6 V													
t <sub>pd</sub>	propagation delay	A to B	1.0	7.9	0.5	5.0	0.5	4.1	0.5	3.1	0.5	2.7	ns
		B to A	1.0	6.8	0.6	4.0	0.5	3.5	0.5	2.9	0.5	2.7	ns
t <sub>dis</sub>	disable time	DIR to A	1.5	5.2	1.5	5.2	1.5	5.2	1.5	5.2	1.5	5.2	ns
		DIR to B	1.7	7.9	0.7	6.1	0.6	6.1	0.7	4.6	1.7	5.2	ns
t <sub>en</sub>	enable time	DIR to A	-	14.7	-	10.1	-	9.6	-	7.5	-	7.9	ns
		DIR to B	-	13.1	-	10.2	-	9.3	-	8.3	-	7.9	ns

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
t<sub>en</sub> is a calculated value using the formula shown in [Section 13.4 "Enable times"](#)

12. Waveforms

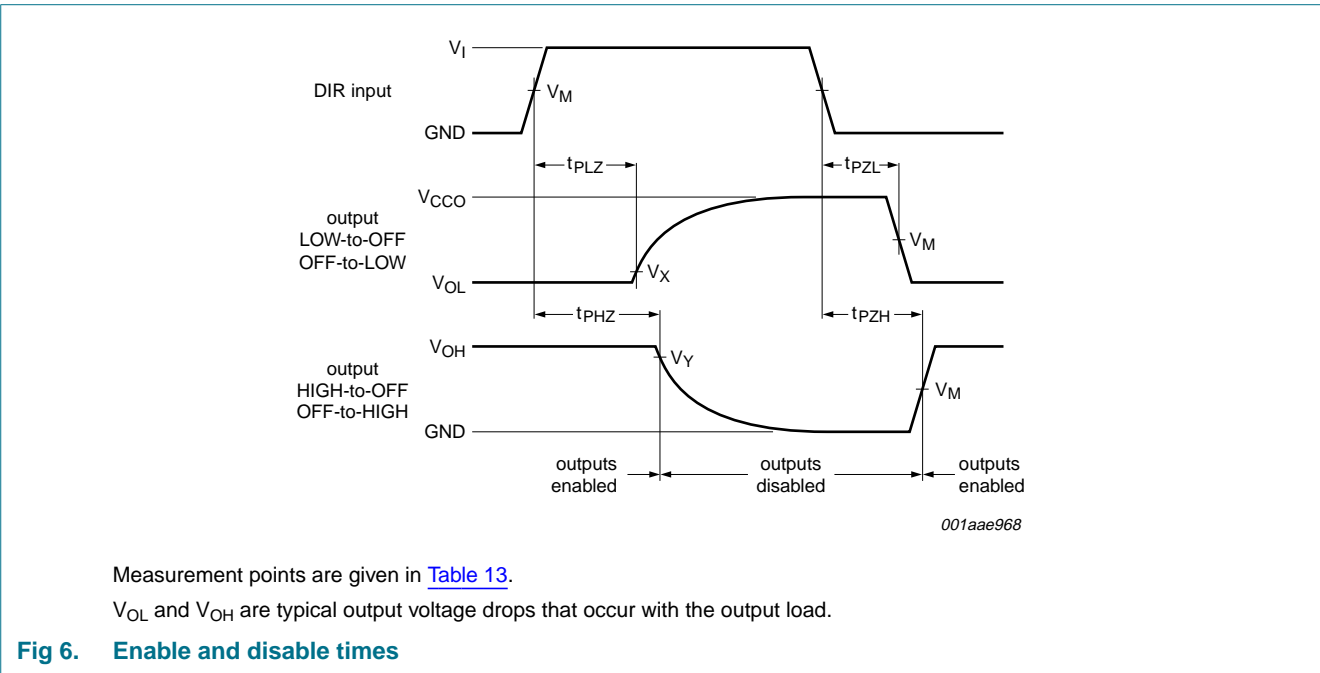
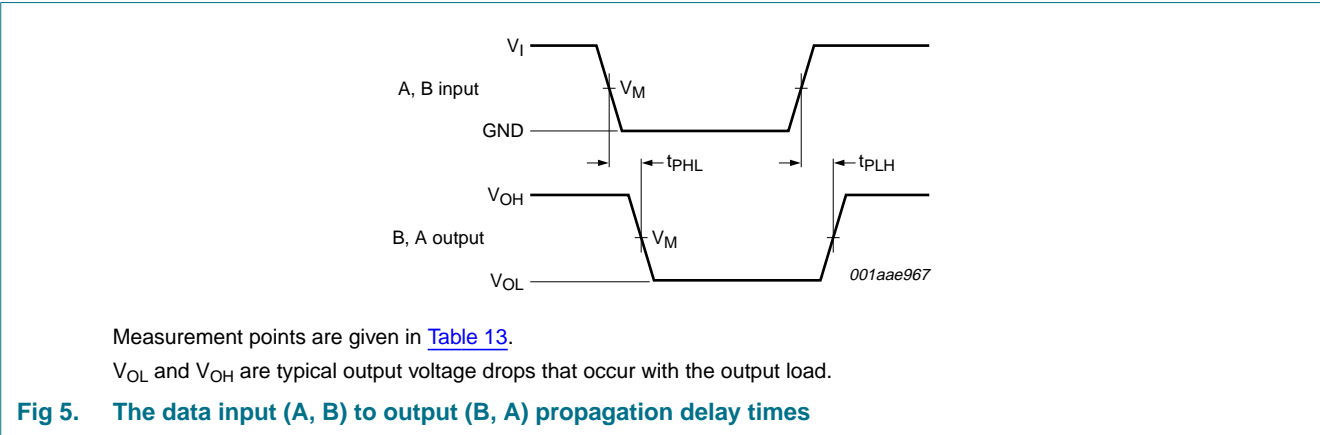


Table 13. Measurement points

Supply voltage	Input <sup>[1]</sup>	Output <sup>[2]</sup>		
$V_{CC(A)}, V_{CC(B)}$	$V_M$	$V_M$	$V_X$	$V_Y$
1.1 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1\text{ V}$	$V_{OH} - 0.1\text{ V}$
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.

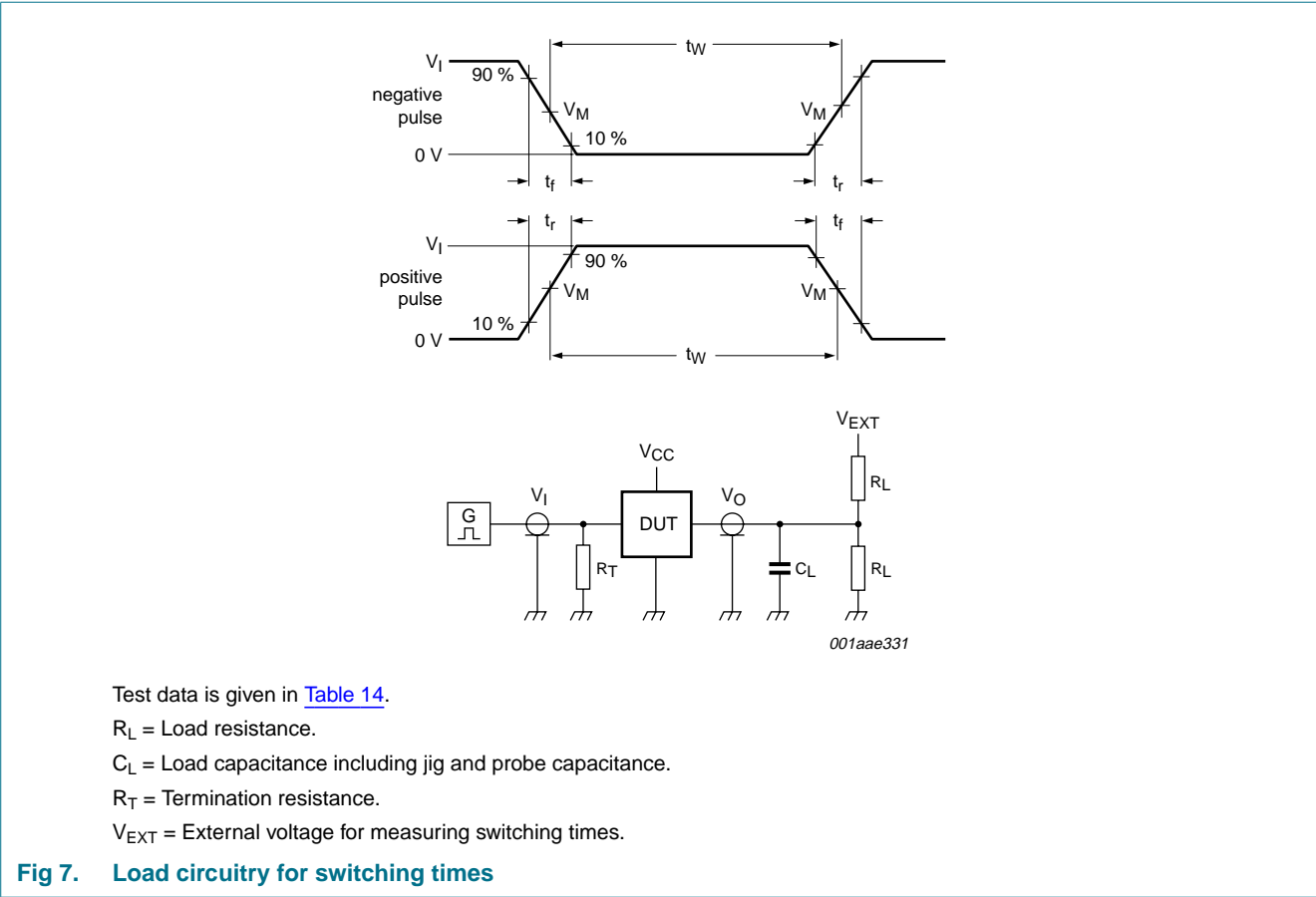


Table 14. Test data

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC(A)}, V_{CC(B)}$	$V_I$ <sup>[1]</sup>	$\Delta t/\Delta V$ <sup>[2]</sup>	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$ <sup>[3]</sup>
1.1 V to 1.6 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.

[2]  $dV/dt \geq 1.0 \text{ V/ns}$

[3]  $V_{CCO}$  is the supply voltage associated with the output port.

13. Application information

13.1 Unidirectional logic level-shifting application

The circuit given in [Figure 8](#) is an example of the 74AVC1T45 being used in an unidirectional logic level-shifting application.

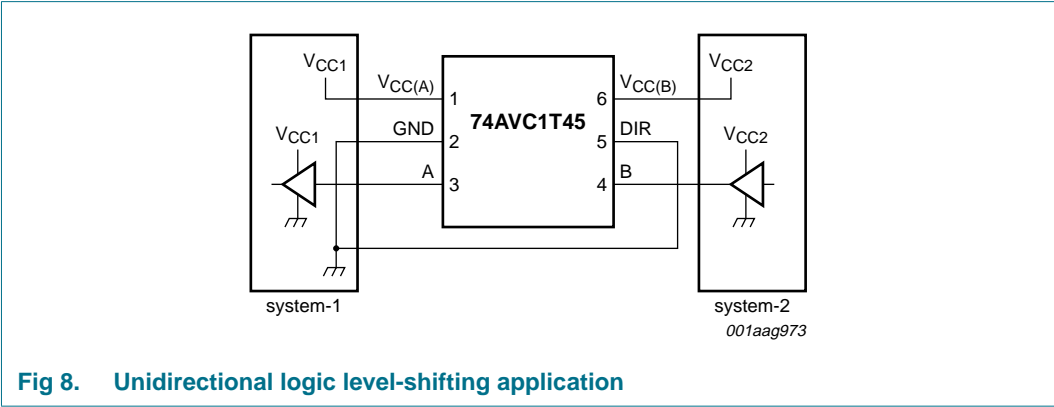
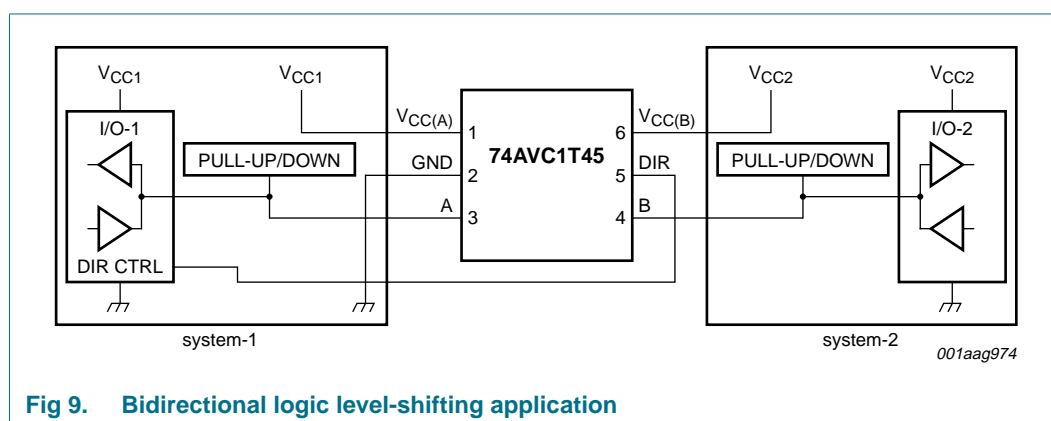


Table 15. Description unidirectional logic level-shifting application

Pin	Name	Function	Description
1	V <sub>CC(A)</sub>	V <sub>CC1</sub>	supply voltage of system-1 (0.8 V to 3.6 V)
2	GND	GND	device GND
3	A	OUT	output level depends on V <sub>CC1</sub> voltage
4	DIR	DIR	the GND (LOW level) determines B port to A port direction
5	B	IN	input threshold value depends on V <sub>CC2</sub> voltage
6	V <sub>CC(B)</sub>	V <sub>CC2</sub>	supply voltage of system-2 (0.8 V to 3.6 V)

## 13.2 Bidirectional logic level-shifting application

**Figure 9** shows the 74AVC1T45 being used in a bidirectional logic level-shifting application. Since the device does not have an output enable pin, the system designer should take precautions to avoid bus contention between system-1 and system-2 when changing directions.



### Fig 9. Bidirectional logic level-shifting application

[Table 16](#) gives a sequence that will illustrate data transmission from system-1 to system-2 and then from system-2 to system-1.

**Table 16. Description bidirectional logic level-shifting application<sup>[1]</sup>**

State	DIR CTRL	I/O-1	I/O-2	Description
1	H	output	input	system-1 data to system-2
2	H	Z	Z	system-2 is getting ready to send data to system-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold.
3	L	Z	Z	DIR bit is set LOW. I/O-1 and I/O-2 still are disabled. The bus-line state depends on bus hold.
4	L	input	output	system-2 data to system-1

[1] H = HIGH voltage level;  
L = LOW voltage level;  
Z = high-impedance OFF-state.

### 13.3 Power-up considerations

The device is designed such that no special power-up sequence is required other than GND being applied first.

**Table 17. Typical total supply current ( $I_{CC(A)} + I_{CC(B)}$ )**

$V_{CC(A)}$	$V_{CC(B)}$							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	$\mu A$
0.8 V	0.1	0.1	0.1	0.1	0.1	0.7	2.3	$\mu A$
1.2 V	0.1	0.1	0.1	0.1	0.1	0.3	1.4	$\mu A$
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.9	$\mu A$
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.5	$\mu A$
2.5 V	0.1	0.7	0.3	0.1	0.1	0.1	0.1	$\mu A$
3.3 V	0.1	2.3	1.4	0.9	0.5	0.1	0.1	$\mu A$

### 13.4 Enable times

Calculate the enable times for the 74AVC1T45 using the following formulas:

- $t_{en} \text{ (DIR to A)} = t_{dis} \text{ (DIR to B)} + t_{pd} \text{ (B to A)}$
- $t_{en} \text{ (DIR to B)} = t_{dis} \text{ (DIR to A)} + t_{pd} \text{ (A to B)}$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the 74AVC1T45 initially is transmitting from A to B, then the DIR bit is switched, the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.



14. Package outline

Plastic surface-mounted package; 6 leadsSOT363

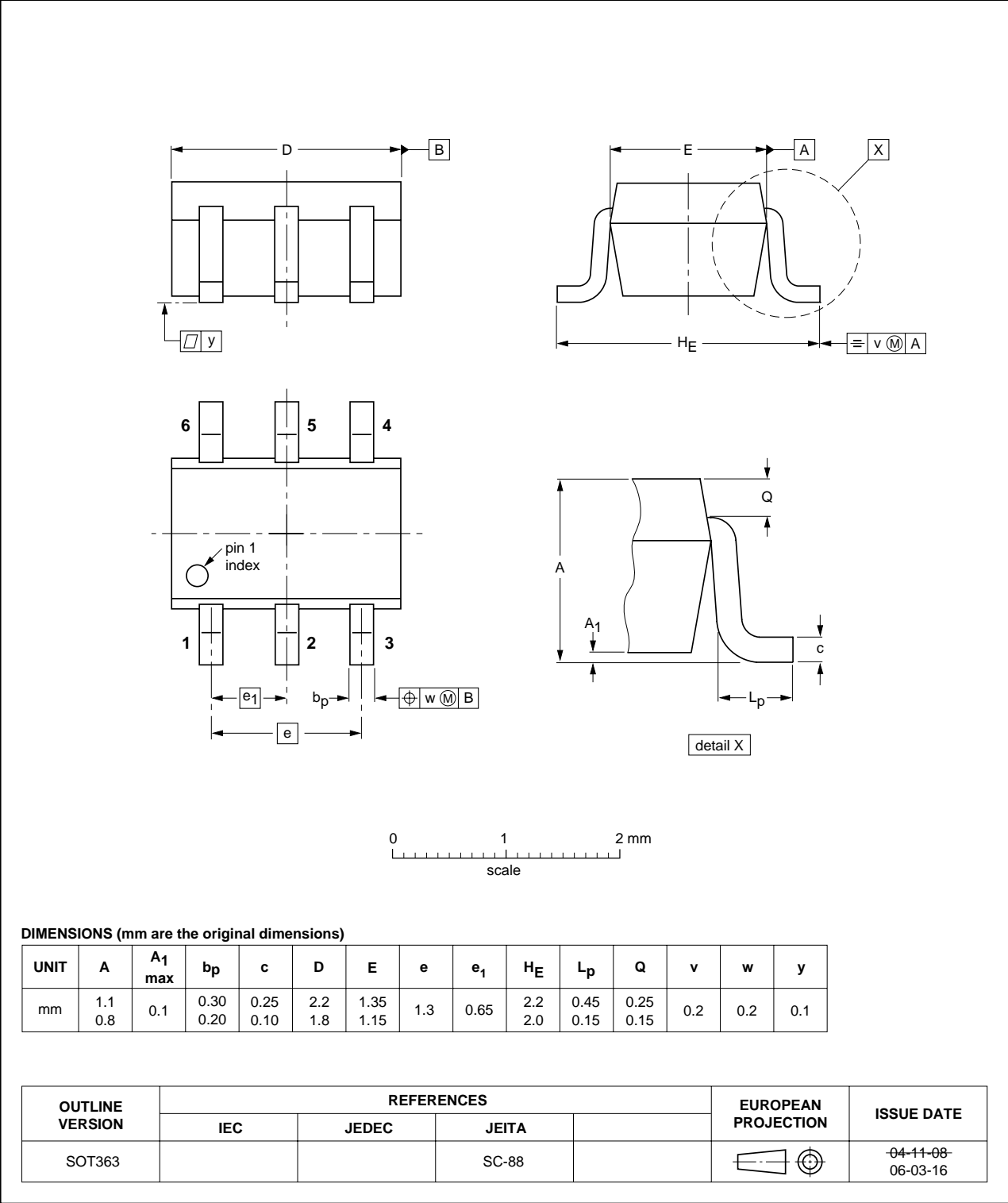


Fig 10. Package outline SOT363 (SC-88)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

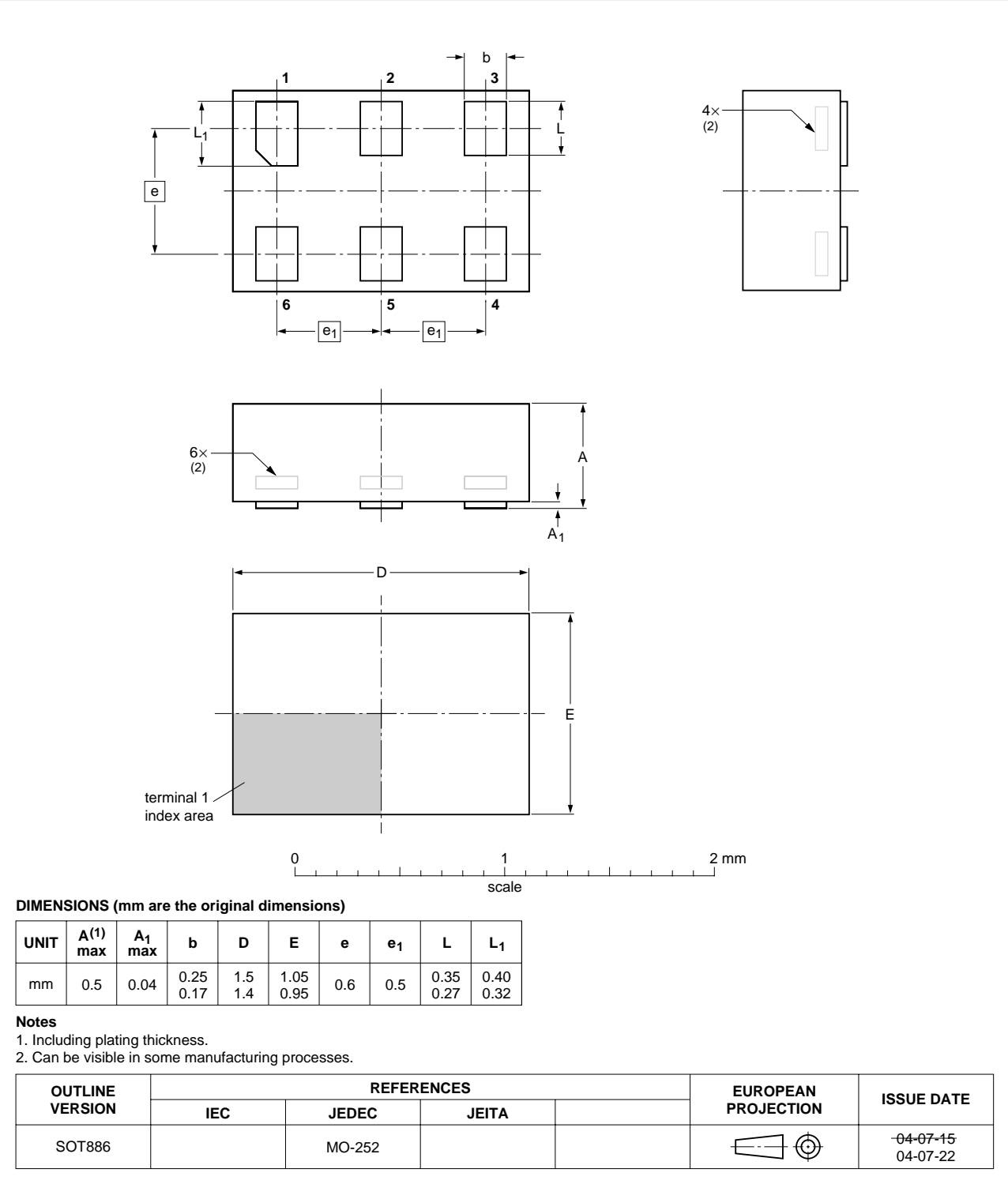


Fig 11. Package outline SOT886 (XSON6)

## 15. Abbreviations

Table 18. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 16. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC1T45_2	20090505	Product data sheet	-	74AVC1T45_1
Modifications:	• Conditions for I <sub>CC</sub> changed			
74AVC1T45_1	20080118	Product data sheet	-	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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