LOW SKEW, 1-TO-24 DIFFERENTIAL-TO-3.3V, 2.5V LVPECL FANOUT BUFFER

ICS853S024

General Description

The ICS853S024 is a low skew, 1-to-24 Differential-to-3.3V, 2.5V LVPECL Fanout Buffer and a member of theHiPerClockS™ family of High Performance Clock Solutions from IDT. The CLK, nCLK pair can accept most standard differential input levels. The ICS853S024 is characterized to operate from either a 3.3V or a 2.5V power supply. Guaranteed output skew characteristics make the ICS853S024 ideal for those clock distribution applications demanding well defined performance and repeatability.

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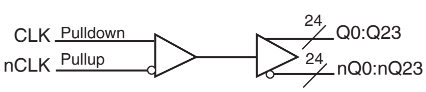
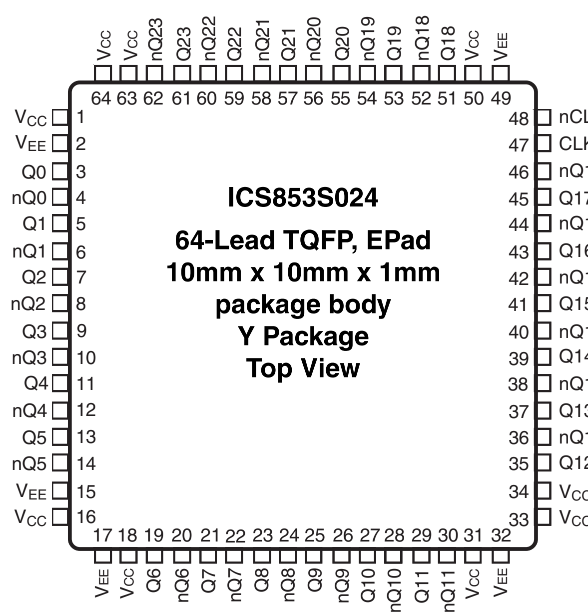
Features

- Twenty four LVPECL outputs.
- One differential clock input pair
- Differential input clock (CLK, nCLK) can accept the following signaling levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency: >1.5GHz
- Translates any single ended input signal to 3.3V/ 2.5V LVPECL levels with resistor bias on nCLK input
- Output skew: 25ps (typical)
- t_R / t_F: 180ps (typical)
- Additive phase jitter, RMS: 0.111ps (typical) @ 312.5MHz
- Full 3.3V or 2.5V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) packages.

Block Diagram



Pin Assignment



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 16, 18, 31, 33, 34, 50, 63, 64	V_{CC}	Power		Power supply pins.
2, 15, 17, 32, 49	V_{EE}	Power		Negative supply pins.
3, 4	Q0, nQ0	Output		Differential clock outputs. LVPECL interface levels.
5, 6	Q1, nQ1	Output		Differential clock outputs. LVPECL interface levels.
7, 8	Q2, nQ2	Output		Differential clock outputs. LVPECL interface levels.
9, 10	Q3, nQ3	Output		Differential clock outputs. LVPECL interface levels.
11, 12	Q4, nQ4	Output		Differential clock outputs. LVPECL interface levels.
13, 14	Q5, nQ5	Output		Differential clock outputs. LVPECL interface levels.
19, 20	Q6, nQ6	Output		Differential clock outputs. LVPECL interface levels.
21, 22	Q7, nQ7	Output		Differential clock outputs. LVPECL interface levels.
23, 24	Q8, nQ8	Output		Differential clock outputs. LVPECL interface levels.
25, 26	Q9, nQ9	Output		Differential clock outputs. LVPECL interface levels.
27, 28	Q10, nQ10	Output		Differential clock outputs. LVPECL interface levels.
29, 30	Q11, nQ11	Output		Differential clock outputs. LVPECL interface levels.
35, 36	Q12, nQ12	Output		Differential clock outputs. LVPECL interface levels.
37, 38	Q13, nQ13	Output		Differential clock outputs. LVPECL interface levels.
39, 40	Q14, nQ14	Output		Differential clock outputs. LVPECL interface levels.
41, 42	Q15, nQ15	Output		Differential clock outputs. LVPECL interface levels.
43, 44	Q16, nQ16	Output		Differential clock outputs. LVPECL interface levels.
45, 46	Q17, nQ17	Output		Differential clock outputs. LVPECL interface levels.
47	CLK	Input	Pulldown	Non-inverting differential clock input.
48	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ default when left floating.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			50		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			50		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	32.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. LVPECL Power Supply DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			200		mA

NOTE 1: Output terminated with 50Ω to V_{CC} / 2. See Parameter Measurement Information Section.

Table 3B. Differential DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK				150	µA
		nCLK				150	µA
I_{IL}	Input Low Current	CLK		-5			µA
		nCLK		-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 3C. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} – 1.4		V_{CC} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} – 2.0		V_{CC} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 3D. LVPECL DC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} – 1.4$		$V_{CC} – 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} – 2.0$		$V_{CC} – 1.5$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

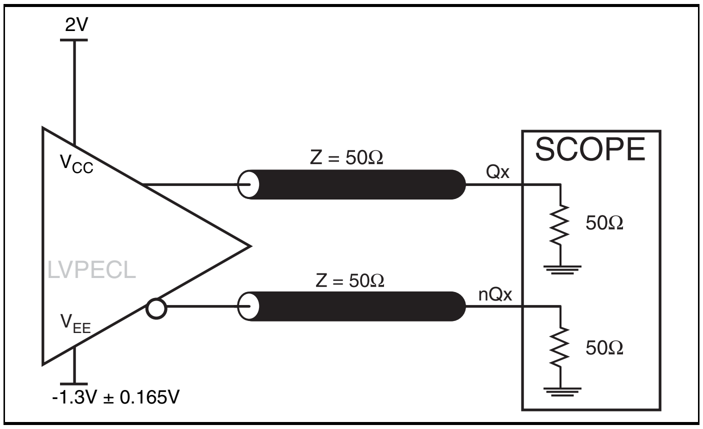
AC Electrical Characteristics

Table 4. AC Characteristics, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

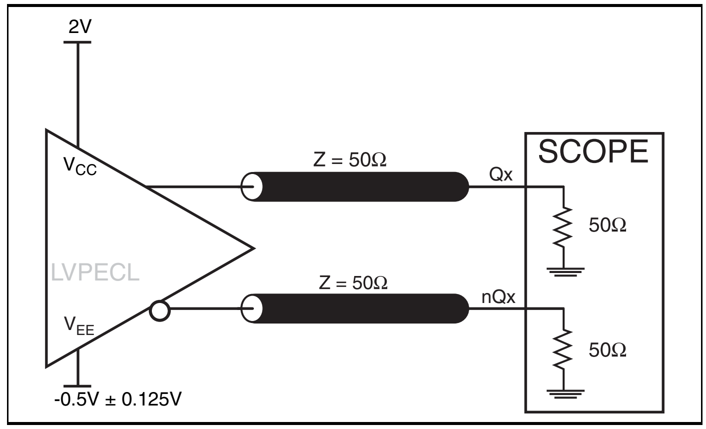
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				1.9	GHz
t_{PD}	Propagation Delay; NOTE 1			600		ps
tjit(ϕ)	Additive Phase Jitter, RMS; NOTE 2	156.25 MHz, Integration Range: 12kHz – 20MHz		0.149		ps
		312.5 MHz, Integration Range: 12kHz – 20MHz		0.111		ps
		1GHz, Integration Range: 12kHz – 20MHz		0.44		ps
tsk(o)	Output Skew; NOTE 3, 4			25		ps
tsk(pp)	Part-to-Part Skew; NOTE 4, 5			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		180		ps
odc	Output Duty Cycle			50		%

All parameters are measured at f ≤ 1GHz, unless otherwise noted.
Special thermal considerations may be required. See Applications Section.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Measured on Aeroflex PN9000.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65. Measured at the output differential cross points.
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions at the same temperature. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

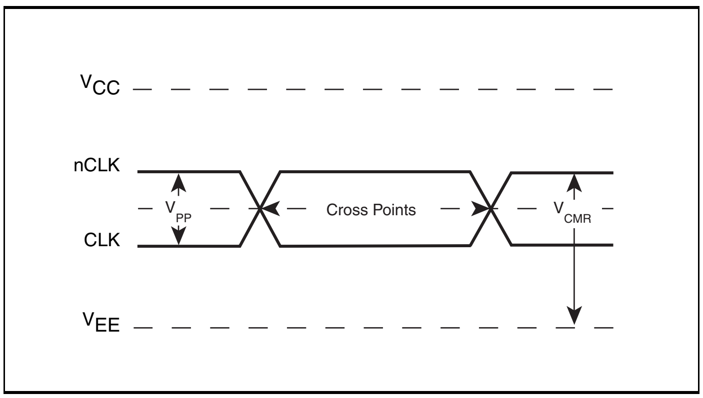
Parameter Measurement Information



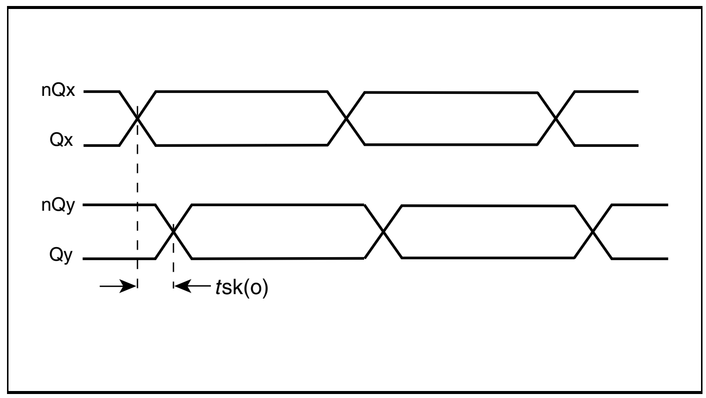
3.3V LVPECL Output Load AC Test Circuit



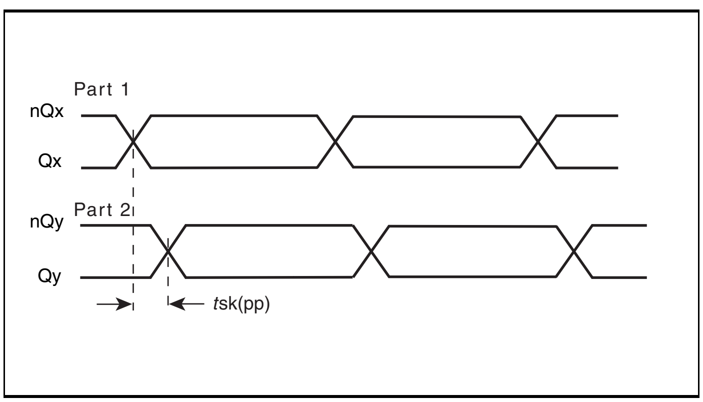
2.5V LVPECL Output Load AC Test Circuit



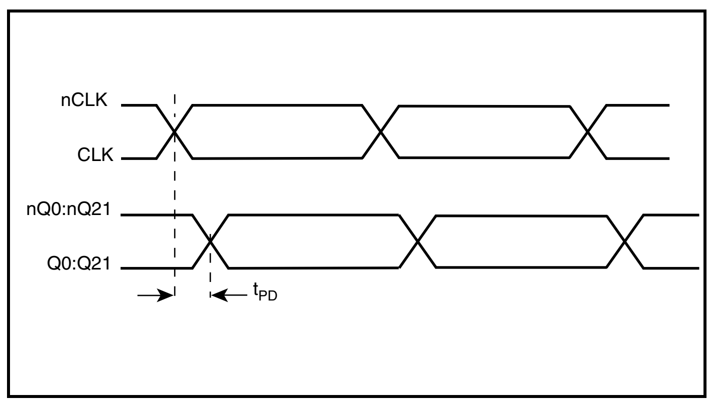
Differential Input Level



Output Skew

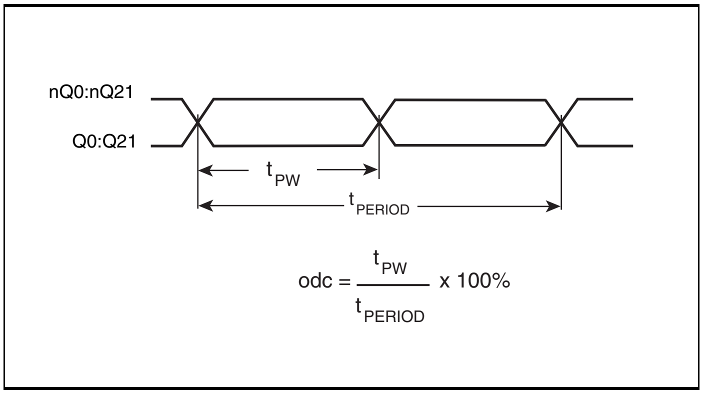


Part-to-Part Skew

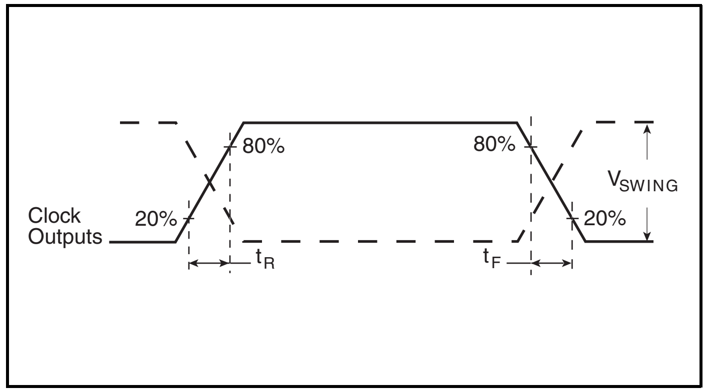


Propagation Delay

Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

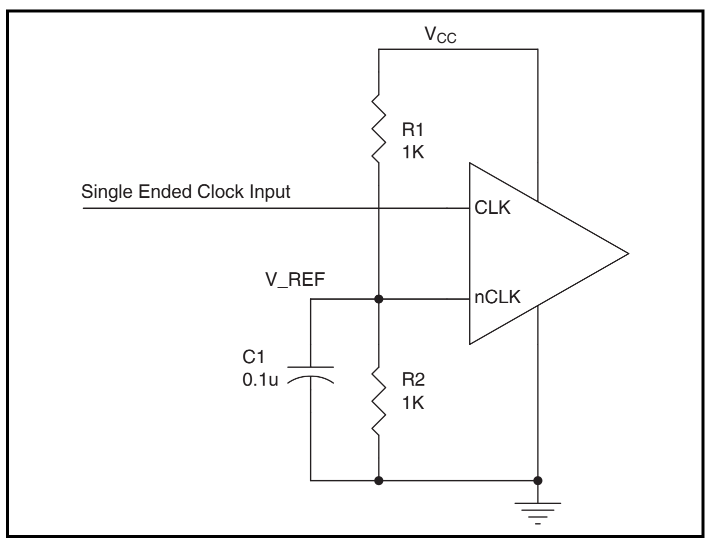


Figure 1. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

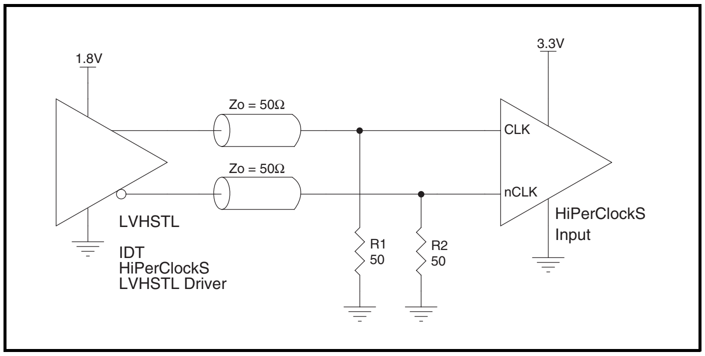


Figure 2A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

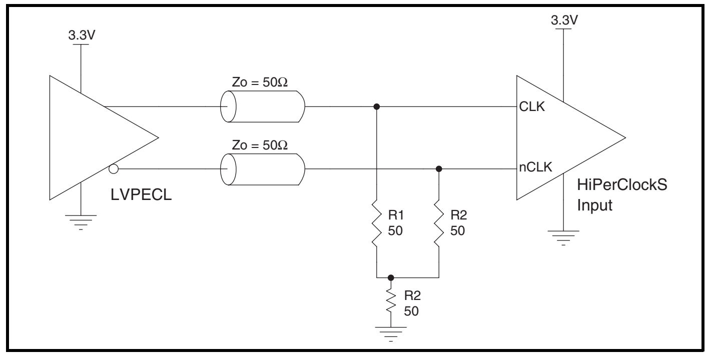


Figure 2B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

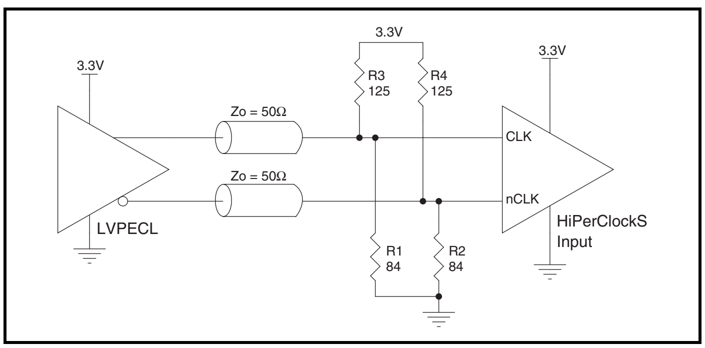


Figure 2C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

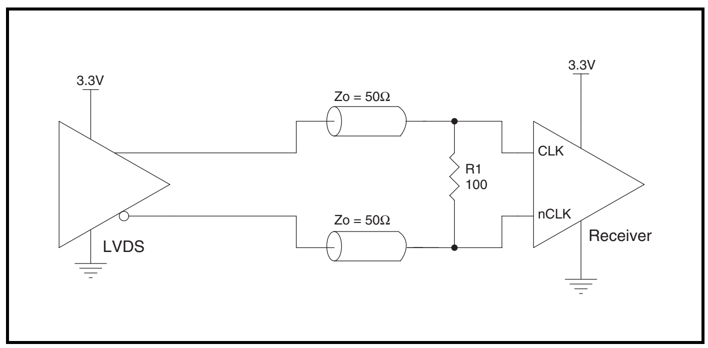


Figure 2D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

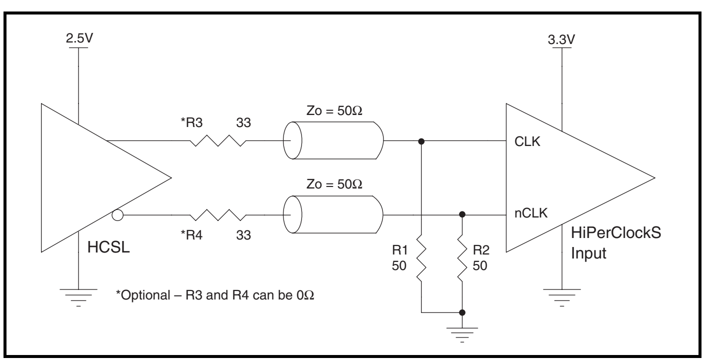


Figure 2E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

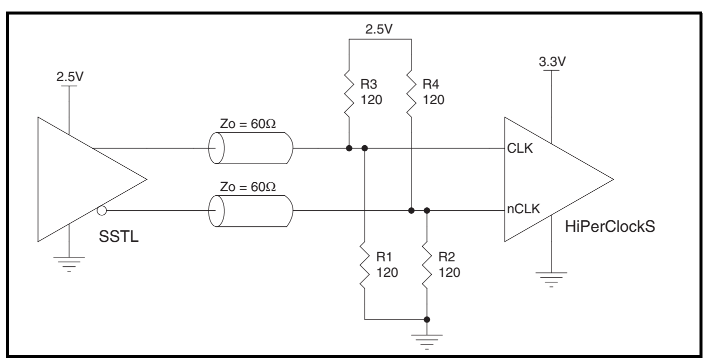


Figure 2F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

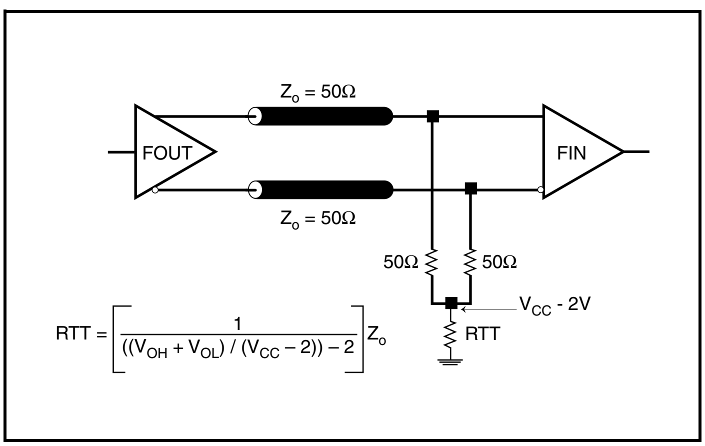


Figure 3A. 3.3V LVPECL Output Termination

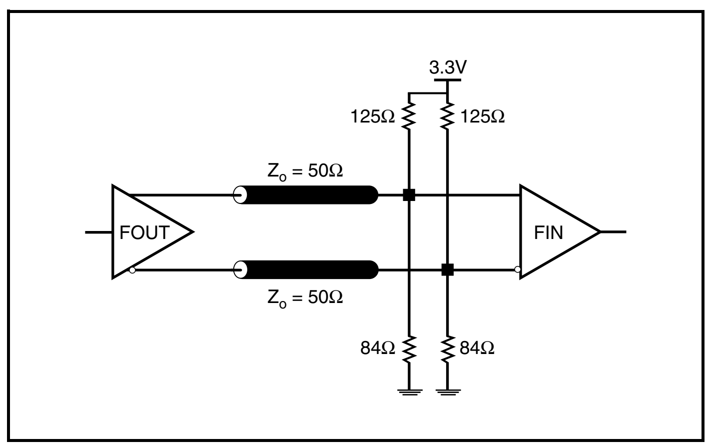


Figure 3B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

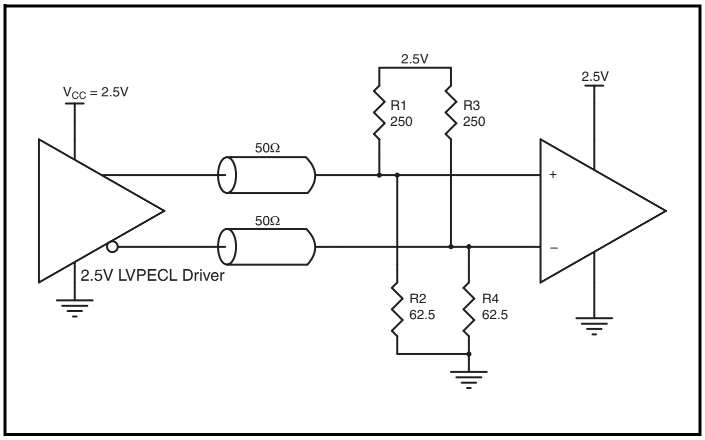


Figure 4A. 2.5V LVPECL Driver Termination Example

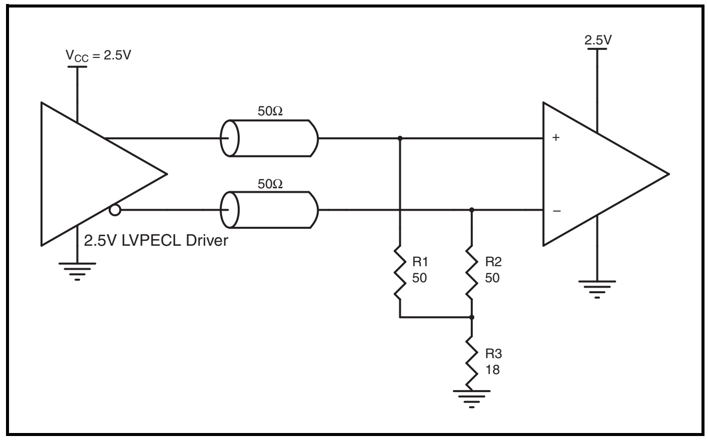


Figure 4B. 2.5V LVPECL Driver Termination Example

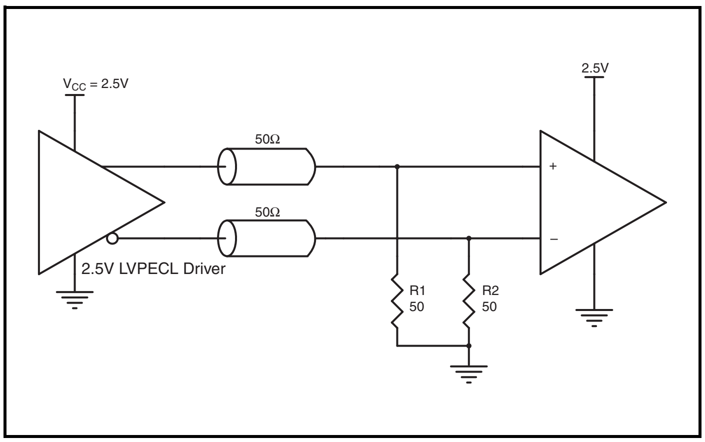


Figure 4C. 2.5V LVPECL Driver Termination Example

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

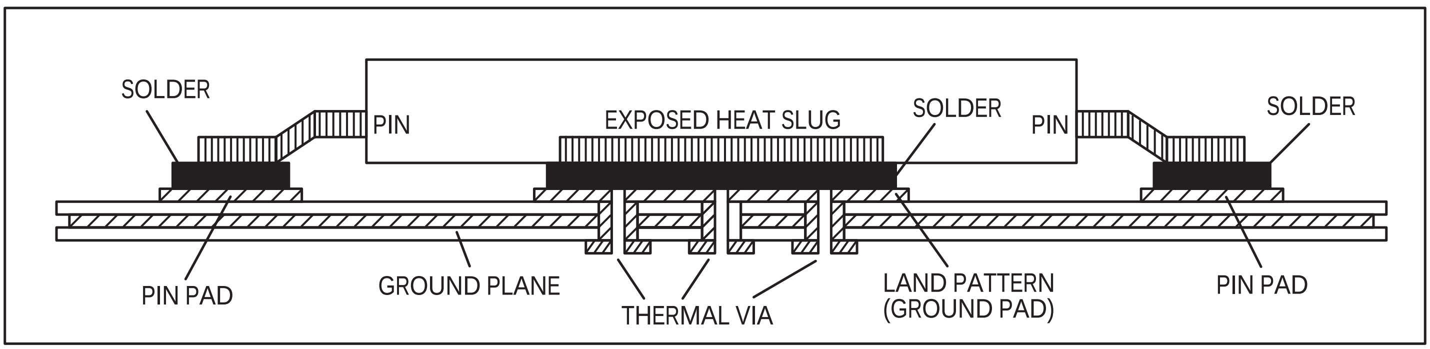


Figure 5. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS853S024.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS853S024 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 200mA = **693mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 24 * 30mW = **720mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 693W + 720mW = **1.413W**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming 0 air flow and a multi-layer board, the appropriate value is 32.5°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 1.413 W * 32.5°C/W = 115.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 5. Thermal Resistance θ_{JA} for 64 Lead TQFP, EPad, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.5°C/W	26.6°C/W	25.1°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

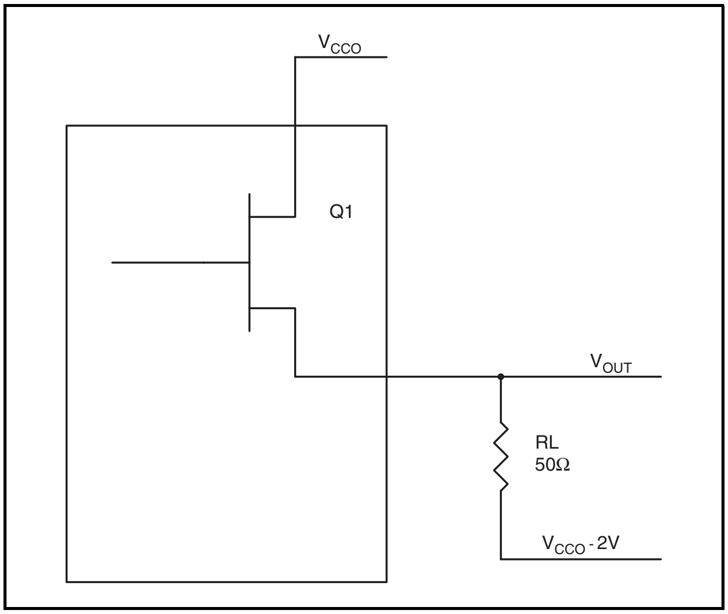


Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

Pd_L = $[(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 64 Lead TQFP, E-Pad

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.5°C/W	26.6°C/W	25.1°C/W

Transistor Count

The transistor count for ICS853S024 is: 8336

Package Outline and Package Dimensions

Package Outline - Y Suffix for 64 Lead TQFP, E-Pad

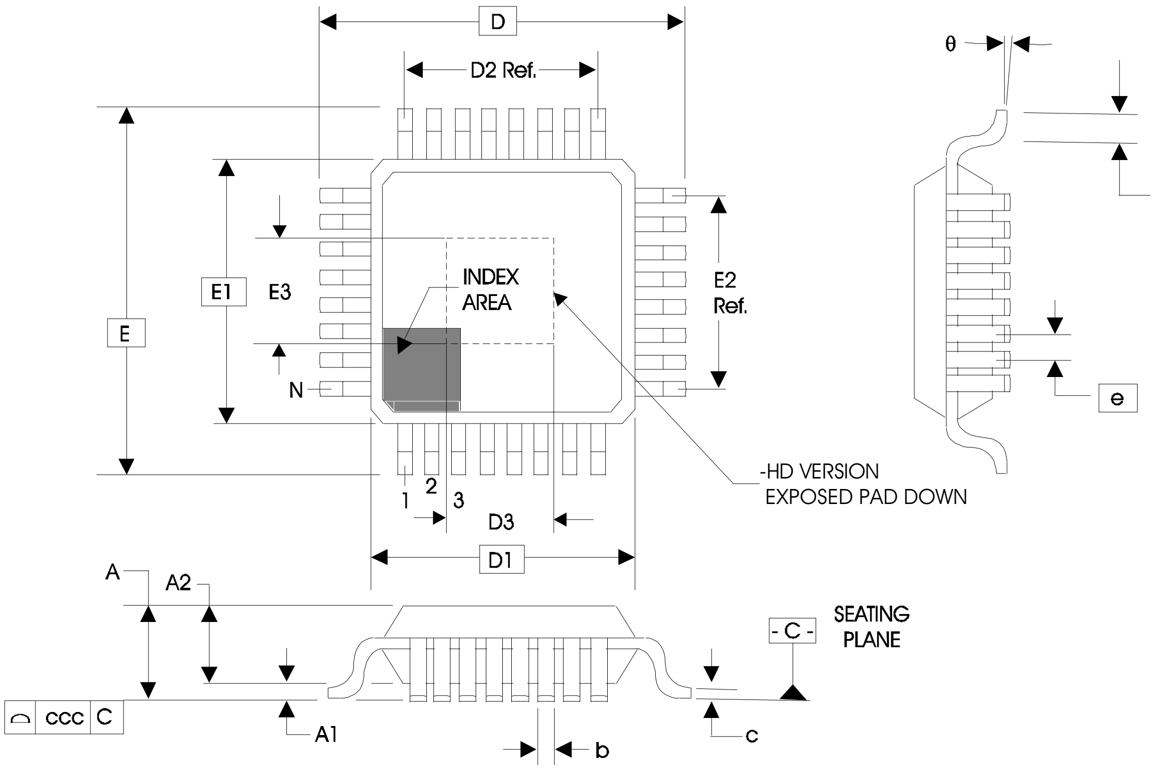


Table 7. Package Dimensions for 64 Lead TQFP, E-Pad

JEDEC Variation: ACD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		64	
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D & E		12.00 Basic	
D1 & E1		10.00 Basic	
D2 & E2		7.50 Ref.	
D3 & E3	4.5	5.0	5.5
e		0.50 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 7. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
853S024AYLF	ICS853S024AYLF	Lead-Free, 64 Lead TQFP, E-Pad	Tray	0°C to +70°C
853S024AYLFT	ICS853S024AYLF	Lead-Free, 64 Lead TQFP, E-Pad	500 Tape & Reel	0°C to +70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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